



Solid State Devices, Inc.

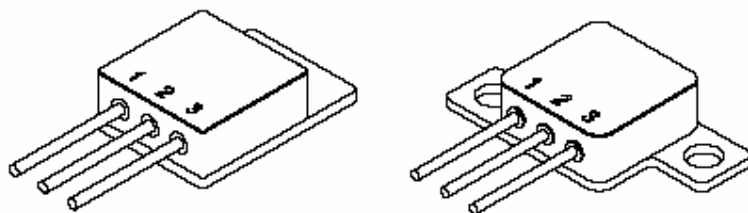
14830 Valley View Blvd * La Mirada, Ca 90638

Phone: (562) 404-7855 * Fax: (562) 404-1773

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DESIGNER'S DATA SHEET

TO-254 and TO-254Z



note 1: Drain Current is package limited

SFF35N20M SFF35N20Z

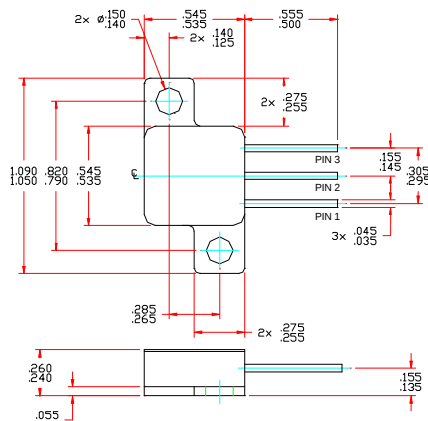
55 AMP (note 1) /200 Volts
35 mO
N-Channel Trench Gate
MOSFET

Features:

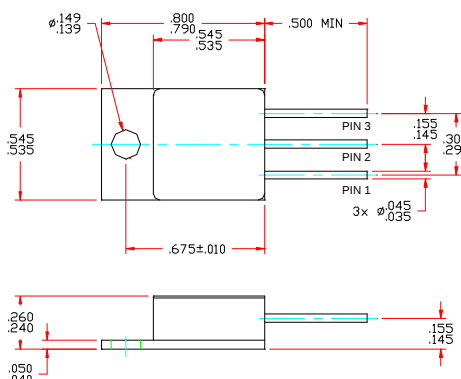
- TRENCH GATE technology
- Lowest ON-resistance in the industry
- UIS rated
- Hermetically Sealed, Isolated Power Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit
- Enhanced replacement for IRHM250 types

Maximum Ratings	Symbol	Value	Units
Drain - Source Voltage	V_{DS}	200	V
Gate – Source Voltage	V_{GS}	± 20	V
Max. Continuous Drain Current (junction temperature limited)	I_{D1} I_{D2}	85 12	A
Max. Continuous Drain Current (package limited)	I_{D3}	55	A
Max. Avalanche current	I_{AR}	35	A
Repetitive Avalanche Energy	E_{AR}	60	mJ
Total Power Dissipation	P_D	210	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +175	°C
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	0.7 (typ 0.55)	°C/W

TO-254Z(Z)



TO-254 (M)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0018A

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SFRC35N20M

SFRC35N20Z

Electrical Characteristics ^{4/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	200	—	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 30A, T_j = 25^\circ C$	$R_{DS(on)}$	—	26	35.0	mO
	$V_{GS} = 10V, I_D = 30A, T_j = 125^\circ C$		—	51	—	
	$V_{GS} = 10V, I_D = 30A, T_j = 175^\circ C$		—	67	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	2.0	—	4.0	V
Gate to Source Leakage	$V_{GS} = \pm 20V$	I_{GSS}	—	—	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 200V, V_{GS} = 0V, T_j = 25^\circ C$	I_{DSS}	—	—	1	μA
	$V_{DS} = 200V, V_{GS} = 0V, T_j = 125^\circ C$		—	—	50	μA
	$V_{DS} = 200V, V_{GS} = 0V, T_j = 175^\circ C$		—	—	250	μA
Forward Transconductance	$V_{DS} = 10V, I_D = 30A, T_j = 25^\circ C$	g_{fs}	23	—	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	90	135	nC
Gate to Source Charge	$V_{DS} = 100V$	Q_{gs}	—	25	—	
Gate to Drain Charge	$I_D = 65A$	Q_{gd}	—	35	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	25	40	nsec
Rise Time	$V_{DS} = 100V$	t_r	—	225	340	
Turn off Delay Time	$I_D = 65A$	$t_{d(off)}$	—	50	75	
Fall Time	$R_G = 2.5O \text{ min}$	t_f	—	200	300	
Diode Forward Voltage	$I_F = 65A, V_{GS} = 0V$	V_{SD}	—	1.0	1.50	V
Diode Reverse Recovery Time	$I_F = 50A, di/dt = 100A/\mu sec$	t_{rr}	—	140	220	nsec
Peak Reverse Recovery Current		$I_{RM(rec)}$	—	8	12.5	A
Reverse Recovery Charge		Q_{rr}	—	0.55	1.3	μC
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	5100	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	480	—	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	210	—	

NOTES:

* Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

1/ For Ordering Information, Price, and Availability Contact Factory.

2/ Screening per MIL-PRF-19500.

3/ For Package Outlines / lead bending options / pinout configurations Contact Factory.

4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

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