



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4470 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF9250

Screening ^{2/}

— = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Package

S1 = SMD1

SFF9250S1

-25 AMP

**Radiation Tolerant
P-Channel POWER MOSFET**

-200 Volts

180 mΩ typ

Features:

- Rugged Construction with Poly Silicon Gate
- Low RDS(on) and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dv/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed
- TX, TXV, and Space Level Screening Available
- Replaces 2N7237U and IRF9250 Types

Maximum Ratings ^{3/}	Symbol	Value	Unit
Drain – Source Voltage	V _{DS}	-200	V
Gate – Source Voltage	V _{GS}	+20	V
Drain Current	I _{D1} I _{D2}	-25	A
		-15	
Pulsed Drain Current (construction limited) T _C = 25°C	I _{D3}	-110	A
Operating & Storage Temperature	T _{OP} & T _{STG}	-55 to +150	°C
Thermal Resistance, Junction to Case	R _{θJC}	0.45 (typ 0.25)	°C/W
Total Device Power Dissipation T _C = 25°C	P _D	275	W
Single Pulse Avalanche Energy	E _{AS}	1000	mJ

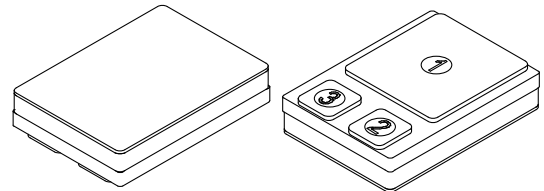
NOTES: *Pulsed per MIL-STD-750.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @ 25°C.

SMD1 (S1)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0116A

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SFF9250S1

Electrical Characteristics ^{3/}	Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = -1\text{ mA}$)	BV_{DSS}	-200	-230	—	V
Drain to Source On State Resistance ($V_{GS} = -12\text{ V}$) $I_D = -15\text{ A}$ $I_D = -25\text{ A}$	$R_{DS(on)}$	— —	180 190	200 250	mΩ
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = -1.0\text{ mA}$) $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $T_J = -55^\circ\text{C}$	$V_{GS(th)}$	-2.0 -1.5 —	-3.2 -2.6 -3.4	-4.0 — -4.5	V
Forward Transconductance ($V_{DS} = -15\text{ V}$, $I_D = -14\text{ A}$)	g_{fs}	11	14	—	S
Zero Gate Voltage Drain Current ($V_{DS} = -100\text{ V}$, $V_{GS} = 0\text{ V}$) ($V_{DS} = -100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	— —	-0.2 -1	-10 -100	μA
Gate to Source Leakage Forward Gate to Source Leakage Reverse $V_{GS} = -20\text{ A}$ $V_{GS} = 20\text{ A}$	I_{GSS}	— —	-5 5	-100 100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge $I_D = -14\text{ A}$ $V_{DS} = -50\text{ V}$ $V_{GS} = -12\text{ V}$	Q_g Q_{gs} Q_{gd}	— — —	100 55 38	125 75 48	nC
Turn on Delay Time Rise Time Turn off Delay Time Fall Time $V_{DD} = -50\text{ V}$ $I_D = -14\text{ A}$ $V_{GS} = -12\text{ V}$	$t_{(on)}$ t_r $t_{d(off)}$ t_f	— — — —	40 70 80 30	60 100 120 50	nsec
Diode Forward Voltage $I_S = -22\text{ A}$ $V_{GS} = 0\text{ V}$ $T_J = 25^\circ\text{C}$	V_{SD}	—	3.05	3.50	V
Diode Reverse Recovery Time Reverse Recovery Charge $T_J = 25^\circ\text{C}$ $I_F = -10\text{ A}$ $di/dt = 100\text{ A}/\mu\text{sec}$	t_{RR} Q_{RR}	— —	280 3.05	350 3.5	nsec μC
Input Capacitance Output Capacitance Reverse Transfer Capacitance $V_{GS} = 0\text{ V}$ $V_{DS} = -25\text{ V}$ $f = 1\text{ MHz}$	C_{iss} C_{oss} C_{rss}	— — —	2300 725 180	— — —	pF

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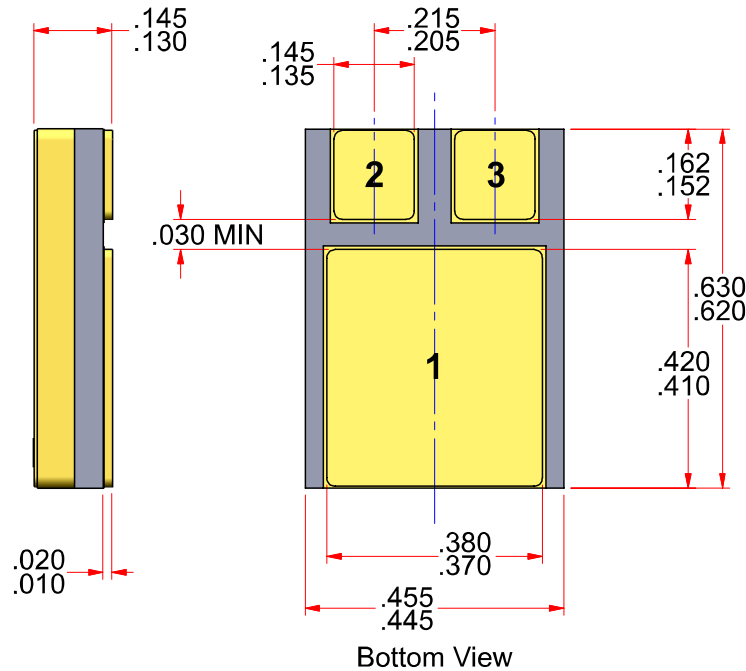


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SFF9250S1

PACKAGE OUTLINE: SMD1 (S1)



Available Part Numbers:

SFF9250S1

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
SMD1 (S1)	Pin 1	Pin 2	Pin 3

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