



Solid State Devices, Inc.

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SFF9240J

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF9240

Screening ^{2/}

___ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Bend Options

___ = Straight Leads
UB = Up Bend
DB = Down Bend

Package

J = TO-257

-11 AMP, -200 Volts, 0.50 Ω P-Channel Power MOSFET

Features:

- Rugged Construction with Poly Silicon Gate
- Low RDS(on) and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dv/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed
- TX, TXV, S-Level Screening Available ^{2/}
- Replacement for IRF9240 Types

Maximum Ratings ^{3/}	Symbol	Value	Unit
Drain to Source Voltage	V _{DS}	-200	V
Gate to Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	-11	A
Single Pulse Avalanche Energy	E _{AS}	500	mJ
Operating & Storage Temperature	T _{OP} & T _{STG}	-55 to +150	°C
Thermal Resistance (Junction to Case)	R _{θJC}	1.7	°C/W
Total Power Dissipation	P _D	73.5 56	W

NOTES: *Pulsed per MIL-STD-750.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @ 25°C.

TO-257 (J)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

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Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	BV_{DSS}	-200	-235	—	V
Drain to Source On State Resistance	$V_{GS} = -10\text{ V}, I_D = -7\text{ A}$	$R_{DS(on)}$	—	0.35	0.50	Ω
	$V_{GS} = -10\text{ V}, I_D = -11\text{ A}$		—	0.38	0.58	
	$V_{GS} = -10\text{ V}, I_D = -11\text{ A}, T_A = 125^\circ\text{C}$		—	0.72	1.10	
On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max}, V_{GS} = 10\text{ V}$	$I_{D(on)}$	-11	—	—	A
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	$V_{GS(th)}$	-2.0	-3.2	-4.0	V
	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}, T_A = 125^\circ\text{C}$		-1.0	-2.7	—	
	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}, T_A = -55^\circ\text{C}$		—	—	-5.0	
Forward Transconductance	$V_{DS} \leq I_{D(on)} \times R_{DS(on)} \text{ max}, I_{DS} = -7\text{ A}$	g_{fs}	4	6	—	S(Ω)
Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	I_{DSS}	—	—	-100	μA
	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}$		—	—	-25	
	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_A = 125^\circ\text{C}$		—	—	-1000	
	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}, T_A = 125^\circ\text{C}$		—	—	-250	
Gate to Source Leakage Forward	$V_{GS} = \pm 20\text{ V}$	I_{GSS}	—	—	± 100	nA
Gate to Source Leakage Reverse	$V_{GS} = \pm 20\text{ V}, T_A = 125^\circ\text{C}$		—	—	± 200	
Total Gate Charge	$V_{GS} = -10\text{ V}$	Q_g	—	22	60	nC
Gate to Source Charge	$V_{DS} = 100\text{ V}$	Q_{gs}	—	8.0	15	
Gate to Drain Charge	$I_D = -11\text{ A}$	Q_{gd}	—	8.0	38	
Turn on Delay Time	$V_{DD} = -100\text{ V}$ $I_D = -6\text{ A}$ $R_G = 4.7\text{ }\Omega$	$t_{d(on)}$	—	33	50	nsec
Rise Time		t_r	—	45	70	
Turn off Delay Time		$t_{d(off)}$	—	73	100	
Fall Time		t_f	—	24	50	
Diode Forward Voltage	$I_S = -11\text{ A}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	V_{SD}	—	-3.0	-5.0	V
Diode Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = -11\text{ A},$	t_{rr}	—	270	440	nsec
Reverse Recovery Charge	$di/dt = 100\text{ A}/\mu\text{sec}$	Q_{rr}	—	2.0	—	μC
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	1200	1300	pF
Output Capacitance	$V_{DS} = 25\text{ V}$	C_{oss}	—	400	500	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	100	250	

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Package	Drain	Source	Gate
TO-257 (J)	1	2	3

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