Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
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SFF9240G

DESIGNER'S DATA SHEET

-11 AMP, -200 Volts, 0.50 Ω P-Channel Power MOSFET

Part Number / Ordering Information 1/

SFF9240 ___ ___

Screening2/
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

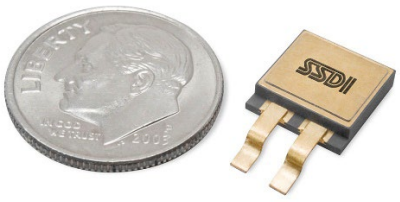
Package
G = Cerpack

Features:
- Rugged Construction with Poly Silicon Gate
- Low RDS(on) and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dv/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed
- TX, TXV, S-Level Screening Available2/
- Replacement for IRF9240 Types

Maximum Ratings3/		Symbol	Value	Unit
Drain to Source Voltage		V_{DS}	-200	**V**
Gate to Source Voltage		V_{GS}	±20	**V**
Continuous Drain Current		I_D	-11	**A**
Single Pulse Avalanche Energy		E_{AS}	500	**mJ**
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	**°C**
Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.6	**°C/W**
Total Power Dissipation	@ T_C = 25°C @ T_C = 55°C	P_D	208 158	**W**

NOTES: *Pulsed per MIL-STD-750.
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @ 25°C.

Cerpack (G)



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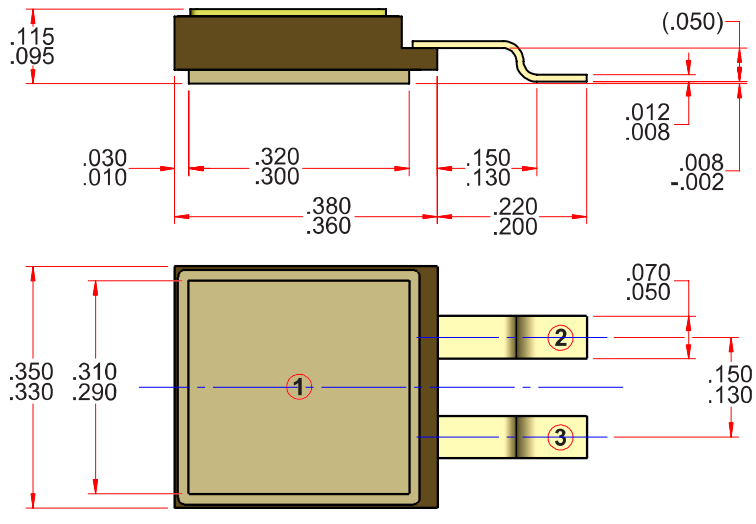
Electrical Characteristics[3/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	BV_{DSS}	-200	-235	—	**V**
Drain to Source On State Resistance	V_{GS} = -10 V, I_D = -7 A V_{GS} = -10 V, I_D = -11 A V_{GS} = -10 V, I_D = -11 A, T_A = 125°C	$R_{DS(on)}$	— — —	0.35 0.38 0.72	0.50 0.58 1.10	**Ω**
On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max, V_{GS} = 10 V	$I_{D(on)}$	-11	—	—	**A**
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA V_{DS} = V_{GS}, I_D = -250 µA, T_A = 125°C V_{DS} = V_{GS}, I_D = -250 µA, T_A = -55°C	$V_{GS(th)}$	-2.0 -1.0 —	-3.2 -2.7 —	-4.0 — -5.0	**V**
Forward Transconductance	V_{DS} = 15 V, I_{DS} = -7 A	g_{fs}	4	6	—	**S(Ʊ)**
Zero Gate Voltage Drain Current	V_{DS} = 200 V, V_{GS} = 0 V V_{DS} = 160 V, V_{GS} = 0 V V_{DS} = 200 V, V_{GS} = 0 V, T_A = 125°C V_{DS} = 160 V, V_{GS} = 0 V, T_A = 125°C	I_{DSS}	— — — —	— — — —	-100 -25 -1000 -250	**µA**
Gate to Source Leakage Forward **Gate to Source Leakage Reverse**	V_{GS} = ±20 V V_{GS} = ±20 V, T_A = 125°C	I_{GSS}	— —	— —	±100 ±200	**nA**
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = -10 V V_{DS} = 100 V I_D = -11 A	Q_g Q_{gs} Q_{gd}	— — —	22 8.0 8.0	60 15 38	**nC**
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{DD} = -100 V V_{GS} = -10 V I_D = -11 A R_G = 4.7 Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	13 45 29 29	50 70 100 50	**nsec**
Diode Forward Voltage	I_S = -11 A, V_{GS} = 0 V, T_J = 25°C	V_{SD}	—	-3.0	-5.0	**V**
Diode Reverse Recovery Time **Reverse Recovery Charge**	T_J = 25°C, I_F = -10 A, di/dt = 100 A/µsec	t_{rr} Q_{rr}	— —	270 2.0	440 —	**nsec** **µC**
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	1200 400 100	1300 500 250	**pF**

CASE OUTLINE: Cerpack (G)



Bottom View

PIN ASSIGNMENT			
Package	**Drain**	**Source**	**Gate**
Cerpack (G)	**1**	**2**	**3**

NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0124A | **DOCX**