Solid State Devices, Inc.
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SFF340-28

DESIGNER'S DATA SHEET

10 AMP, 400 Volts, 0.55 Ω N-Channel Power MOSFET

Part Number / Ordering Information [1/]

SFF340 ____ ____

Screening[2/]
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

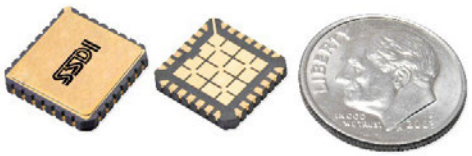
Package
-28 = LCC28

Features:
- Rugged Construction with Poly Silicon Gate
- Low RDS(on) and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dv/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed Surface Mount Package
- TX, TXV, S-Level Screening Available[2/]
- Replacement for IRF340 Types

Maximum Ratings[3/]		Symbol	Value	Unit
Drain to Source Voltage		V_{DS}	400	V
Gate to Source Voltage		V_{GS}	±20	V
Continuous Drain Current	@ T_C = 25°C @ T_C = 100°C	I_{D1} I_{D2}	10 7.2	A
Avalanche Energy (Single Pulse)		E_{AS}	5.7	mJ
Avalanche Current		I_{AR}	10	A
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	°C
Thermal Resistance (Junction to Case)		$R_{\theta JC}$	3.5	°C/W
Total Power Dissipation	@ T_C = 25°C @ T_C = 55°C	P_D	36 27	W

NOTES: *Pulsed per MIL-STD-750.
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @ 25°C.

LCC28 (-28)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	DATA SHEET #: F00073B	DOCX

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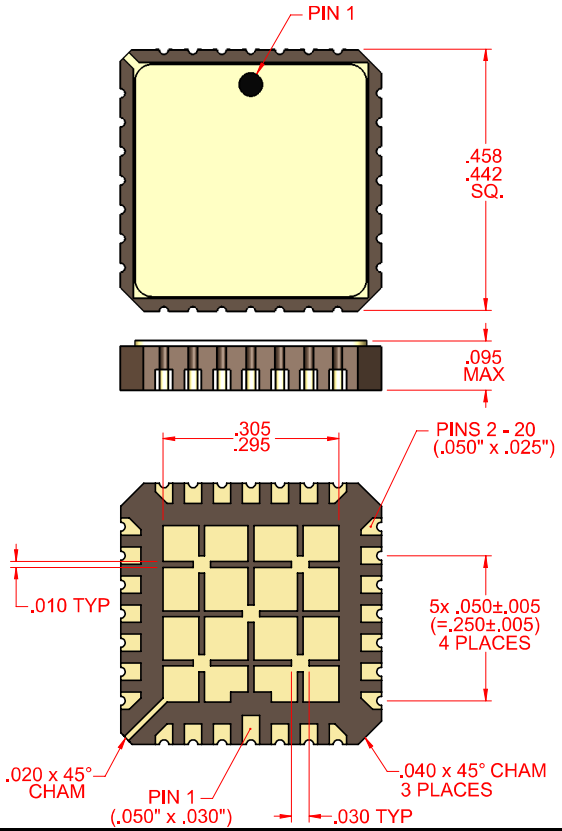
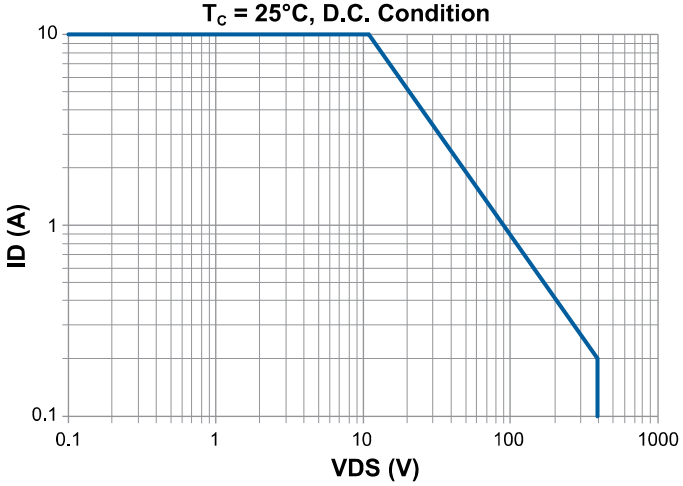
Electrical Characteristics[3/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	BV_{DSS}	400	450	—	V
Drain to Source On State Resistance	V_{GS} = 10 V, I_D = 6 A	$R_{DS(on)}$	—	0.5	0.55	Ω
On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max, V_{GS} = 10 V	$I_{D(on)}$	10	—	—	A
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	2.0	3.2	4.0	V
Forward Transconductance	V_{DS} ≥ 50 V, I_{DS} = 6 A	g_{fs}	5	6	—	S(℧)
Zero Gate Voltage Drain Current	V_{DS} = 400 V, V_{GS} = 0 V V_{DS} = 320 V, V_{GS} = 0 V, T_A = 125°C	I_{DSS}	— —	0.1 1	25 250	µA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V_{GS}	I_{GSS}	— —	1 1	100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V_{GS} = 10 V 80% rated V_{DS} I_D = 10 A	Q_g Q_{gs} Q_{gd}	— — —	25 6 12	50 10 25	nC
Turn on Delay Time Rise Time Turn off Delay Time Fall Time	V_{DD} = 200 V I_D = 10 A V_{GS} = 10 V	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	28 27 75 15	40 60 100 30	nsec
Diode Forward Voltage	I_S = 10 A, V_{GS} = 0 V, T_J = 25°C	V_{SD}	—	—	2.0	V
Diode Reverse Recovery Time Reverse Recovery Charge	T_J = 25°C, I_F = 10 A, di/dt = 100 A/µsec	t_{rr} Q_{rr}	170 1.6	600 6.7	700 8	nsec µC
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	3500 340 90	— — —	pF

CASE OUTLINE: LCC28 (-28)



SFF340-28
SAFE OPERATING AREA
T_C = 25°C, D.C. Condition



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PIN ASSIGNMENT (Standard)			
Package	Drain	Source	Gate
LCC28	5 - 11	1, 15 - 28	2, 3, 13, 14

Note: All Drain / Source Pins must be connected on the PC Board in order to maximize current capability and minimize RDS(on)

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