



Solid State Devices, Inc.

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SFF340J, SFF340M, and SFF340Z

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF340

Screening^{2/}

— = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Lead Bend Options

— = Straight Leads
UB = Up Bend
DB = Down Bend

Package

J = TO-257
M = TO-254
Z = TO-254Z

10 AMP, 400 Volts, 0.55 Ω N-Channel Power MOSFET

Features:

- Rugged Construction with Poly Silicon Gate
- Low RDS(on) and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dv/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed Surface Mount Package
- TX, TXV, S-Level Screening Available^{2/}
- Replacement for IRF340 Types

Maximum Ratings ^{3/}	Symbol	Value	Unit
Drain to Source Voltage	V _{DS}	400	V
Gate to Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _{D1} I _{D2}	10 7.2	A
		@ T _C = 25°C @ T _C = 100°C	
Avalanche Energy (Single Pulse)	E _{AS}	5.7	mJ
Avalanche Current	I _{AR}	10	A
Operating & Storage Temperature	T _{OP} & T _{STG}	-55 to +150	°C
Thermal Resistance (Junction to Case)	R _{θJC}	1.5 1.7	°C/W
		TO-254, TO-254Z TO-257	
Total Power Dissipation	P _D	73.5 56	W
		TO-257 @ T _C = 25°C @ T _C = 55°C	
Total Power Dissipation	P _D	83 63	W
		TO-254 & TO-254Z @ T _C = 25°C @ T _C = 55°C	

NOTES: *Pulsed per MIL-STD-750.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @ 25°C.

TO-257 (J) TO-254 (M) TO-254Z (Z)



NOTE: All specifications are subject to change without notification. SSD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00075D

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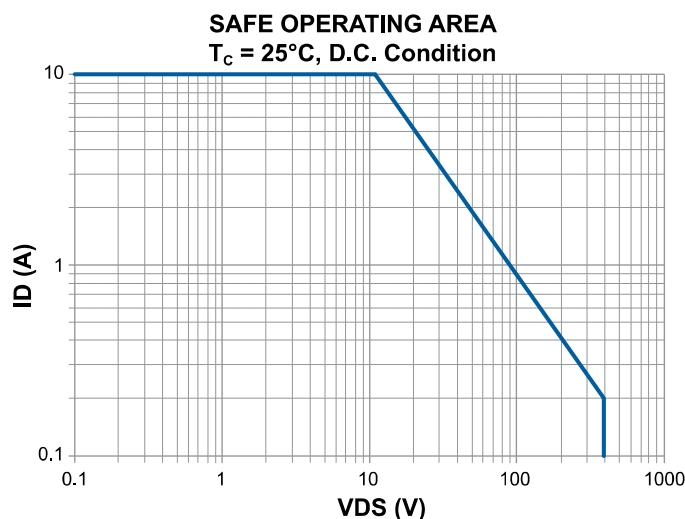


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Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	BV_{DSS}	400	450	—	V
Drain to Source On State Resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	$R_{DS(on)}$	—	0.5	0.55	Ω
On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max}, V_{GS} = 10\text{ V}$	$I_{D(on)}$	10	—	—	A
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	$V_{GS(th)}$	2.0	3.2	4.0	V
Forward Transconductance	$V_{DS} \geq 50\text{ V}, I_{DS} = 6\text{ A}$	g_{fs}	5	6	—	S(O)
Zero Gate Voltage Drain Current	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_A = 125^\circ\text{C}$	I_{DSS}	—	0.1 1	25 250	μA
Gate to Source Leakage Forward	At rated V_{GS}	I_{GSS}	—	1	100	nA
Gate to Source Leakage Reverse			—	1	-100	
Total Gate Charge	$V_{GS} = 10\text{ V}$	Q_g	—	25	50	nC
Gate to Source Charge	80% rated V_{DS}	Q_{gs}	—	6	10	
Gate to Drain Charge	$I_D = 10\text{ A}$	Q_{gd}	—	12	25	
Turn on Delay Time	$V_{DD} = 200\text{ V}$ $I_D = 10\text{ A}$	$t_{d(on)}$	—	28	40	nsec
Rise Time		t_r	—	27	60	
Turn off Delay Time	$V_{GS} = 10\text{ V}$	$t_{d(off)}$	—	75	100	
Fall Time		t_f	—	15	30	
Diode Forward Voltage	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	V_{SD}	—	—	2.0	V
Diode Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 10\text{ A},$	t_{rr}	170	600	700	nsec
Reverse Recovery Charge	$di/dt = 100\text{ A}/\mu\text{sec}$	Q_{rr}	1.6	6.7	8	
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	3500	—	pF
Output Capacitance	$V_{DS} = 25\text{ V}$	C_{oss}	—	340	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	90	—	



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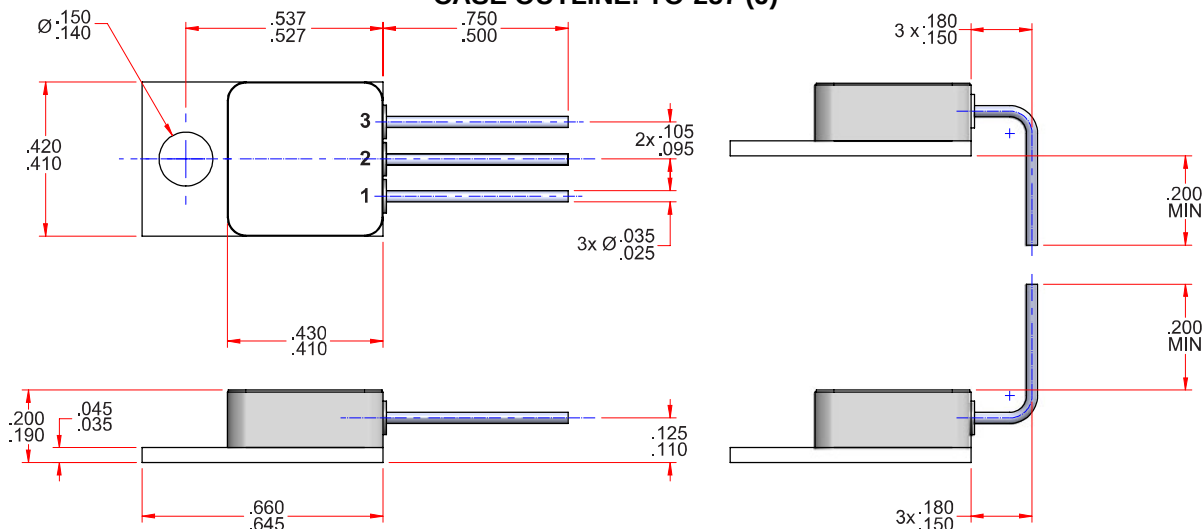
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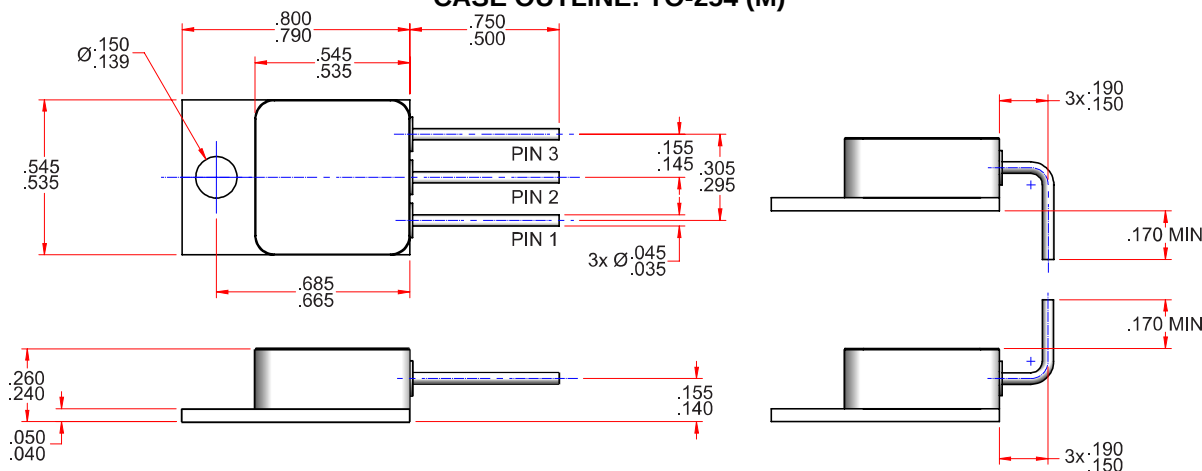
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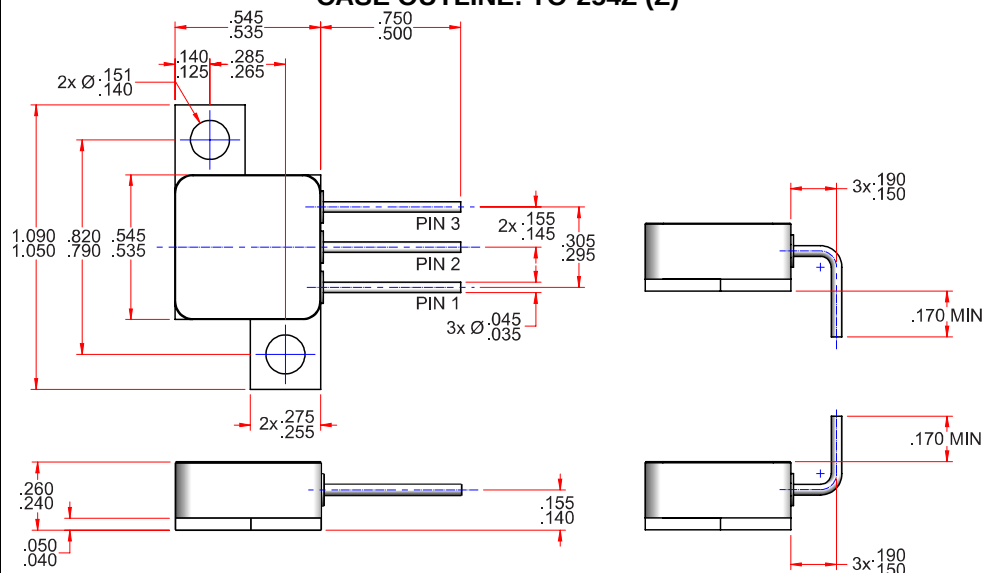
CASE OUTLINE: TO-257 (J)



CASE OUTLINE: TO-254 (M)



CASE OUTLINE: TO-254Z (Z)



PIN ASSIGNMENT

Package	Drain	Source	Gate
TO-257 (J)	1	2	3
TO-254 (M)	1	2	3
TO-254Z (Z)	1	2	3

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