Solid State Devices, Inc.
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SFF440S1

DESIGNER'S DATA SHEET

8 AMP, 500 Volts, 0.85 Ω N-Channel Power MOSFET

Part Number / Ordering Information [1/]

SFF440 ____ ____

Screening[2/]
__ = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

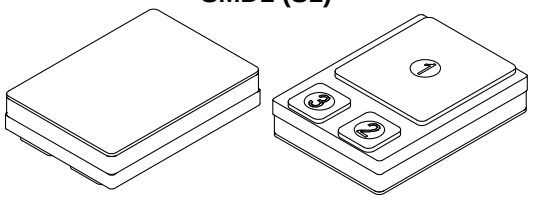
Package
S1 = SMD1

Features:
- Rugged Construction with Poly Silicon Gate
- Low RDS(on) and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dv/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Hermetically Sealed Surface Mount Package
- TX, TXV, S-Level Screening Available[2/]
- Replacement for IRF440 Types

Maximum Ratings[3/]		Symbol	Value	Unit
Drain to Source Voltage		V_{DS}	500	**V**
Gate to Source Voltage		V_{GS}	±20	**V**
Continuous Drain Current	@ 25°C @ 100°C	I_D	8 5	**A**
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	**°C**
Thermal Resistance (Junction to Case)		$R_{\theta JC}$	1.7	**°C/W**
Total Power Dissipation	@ T_C = 25°C @ T_C = 55°C	P_D	74 55	**W**
Single Pulse Avalanche Energy **Repetitive Avalanche Energy**		E_{AS} E_{AR}	3.6 -	**mJ**

NOTES: *Pulsed per MIL-STD-750.
1/ For ordering information, price, and availability - contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ Unless otherwise specified, all electrical characteristics @ 25°C.

SMD1 (S1)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	DATA SHEET #: F00083D	DOCX

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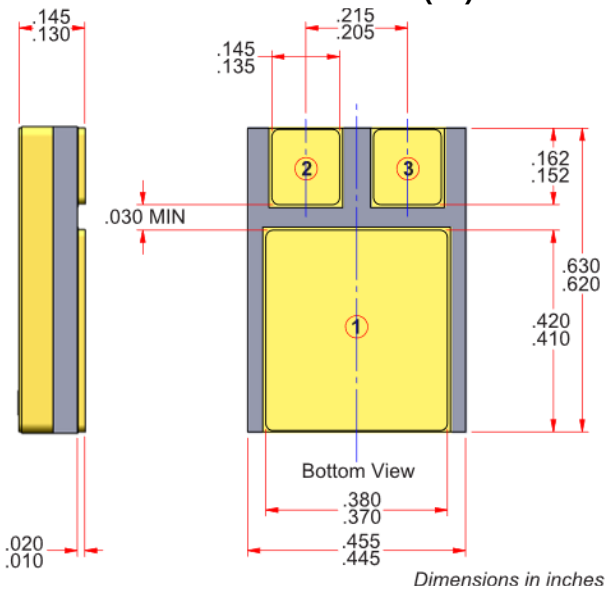
Electrical Characteristics[3/]		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	BV_{DSS}	500	—	—	V
Temperature Coefficient of Breakdown Voltage		$\frac{\Delta BV_{DSS}}{\Delta T_J}$	—	0.78	—	V/°C
Drain to Source On State Resistance	V_{GS} = 10 V, I_D = 5 A V_{GS} = 10 V, I_D = 8 A	$R_{DS(on)}$	— —	0.70 —	0.85 0.98	Ω
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	2.0	—	4.0	V
Forward Transconductance	V_{DS} ≥ 10 V, I_{DS} = 5 A	g_{fs}	4.7	7.4	—	S(Ʊ)
Zero Gate Voltage Drain Current	V_{DS} = 80% rated voltage, V_{GS} = 0 V V_{DS} = 80% rated V_{DS}, V_{GS} = 0 V, T_A = 125°C	I_{DSS}	— —	— —	25 250	µA
Gate to Source Leakage Forward **Gate to Source Leakage Reverse**	At rated V_{GS}	I_{GSS}	— —	— —	100 -100	nA
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10 V 50% rated V_{DS} I_D = 8 A	Q_g Q_{gs} Q_{gd}	27.3 2 11	34 6 17	68.5 12.5 42	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{DD} = 50% rated V_{DS} I_D = 8 A R_G = 9.1 Ω	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	22 27 42 15	45 49 72 51	nsec
Diode Forward Voltage	I_S = rated I_D, V_{GS} = 0 V, T_J = 25°C	V_{SD}	—	—	1.5	V
Diode Reverse Recovery Time **Reverse Recovery Charge**	T_J = 25°C, I_F = rated I_D, di/dt = 100 A/µsec	t_{rr} Q_{rr}	— —	380 3	700 8.9	nsec µC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	1300 310 120	— — —	pF

CASE OUTLINE: SMD1 (S1)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
SMD1	Pin 1	Pin 2	Pin 3

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