



Solid State Devices, Inc.

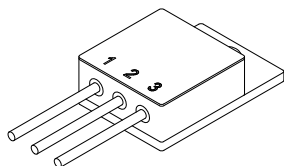
14701 Firestone Blvd * La Mirada, Ca 90638

Phone: (562) 404-4474 * Fax: (562) 404-1773

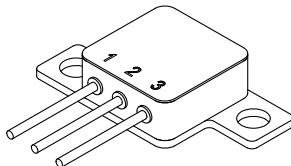
ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

TO-254



TO-254Z



Note 1: maximum current limited by package configuration

SFF23N60M SFF23N60Z

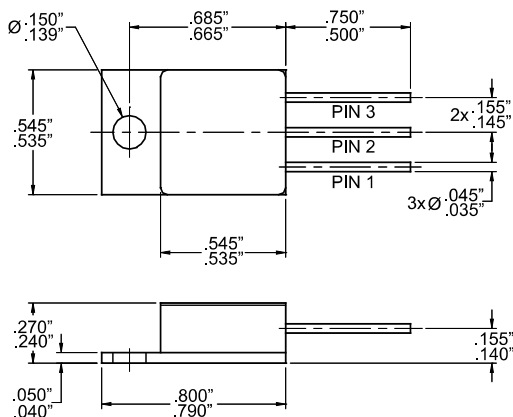
15 AMP, 600 Volts, 320 mΩ Avalanche Rated N-channel MOSFET

Features:

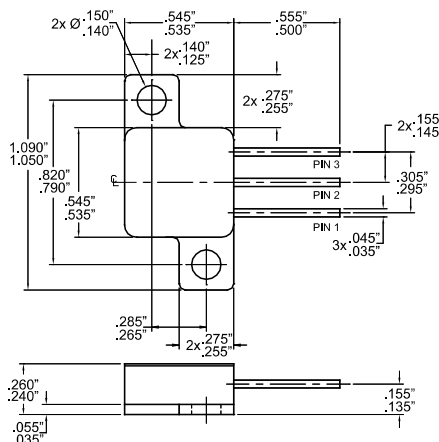
- Advanced low gate charge process
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	600	V
Gate – Source Voltage	continuous	V_{GS}	± 30	V
	transient		± 40	
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ\text{C}$	I_{D1}	15	A
	@ $T_C = 125^\circ\text{C}$	I_{D2}	7	
Max. Instantaneous Drain Current (Tj limited)	@ $T_C = 25^\circ\text{C}$	I_{D3}	23	A
Max. Avalanche current	@ $L = 0.1 \text{ mH}$	I_{AR}	23	A
Single / Repetitive Avalanche Energy	@ $L = 0.1 \text{ mH}$	E_{AS} / E_{AR}	1500 / 30	mJ
Total Power Dissipation	@ $T_C = 25^\circ\text{C}$	P_D	150	W
Operating & Storage Temperature		$T_{OP} \text{ \& } T_{STG}$	-55 to +150	$^\circ\text{C}$
Maximum Thermal Resistance (Junction to Case)		R_{jc}	0.83 (typ.0.6)	$^\circ\text{C/W}$

**TO254
(M)**



**TO254Z
(Z)**



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0028A

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SFF23N60M

SFF23N60Z

Electrical Characteristics ^{4/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	600	620	—	V
Drain to Source On State Resistance	$V_{GS} = 10V, I_D = 11.5A, T_j = 25^\circ C$	$R_{DS(on)}$	—	300	320	mΩ
	$V_{GS} = 10V, I_D = 25A, T_j = 25^\circ C$		—	300	—	
	$V_{GS} = 10V, I_D = 11.5A, T_j = 125^\circ C$		—	670	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 4mA, T_j = 25^\circ C$	$V_{GS(th)}$	2.0	3.5	4.5	V
	$V_{DS} = V_{GS}, I_D = 1mA, T_j = 25^\circ C$		—	3.4	—	
Gate to Source Leakage	$V_{GS} = \pm 30V, T_j = 25^\circ C$	I_{GSS}	—	20	± 100	nA
	$V_{GS} = \pm 20V, T_j = 125^\circ C$		—	30	—	
Zero Gate Voltage Drain Current	$V_{DS} = 600V, V_{GS} = 0V, T_j = 25^\circ C$	I_{DSS}	—	0.1	25	μA
	$V_{DS} = 480V, V_{GS} = 0V, T_j = 125^\circ C$		—	0.085	1	
Forward Transconductance	$V_{DS} = 10V, I_D = 11.5A, T_j = 25^\circ C$	g_{fs}	10	20	—	Mho
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	100	—	nC
Gate to Source Charge	$V_{DS} = 300V$	Q_{gs}	—	23	—	
Gate to Drain Charge	$I_D = 16.5A$	Q_{gd}	—	45	—	
Turn on Delay Time	$V_{GS} = 10V$	$t_{d(on)}$	—	28	—	nsec
Rise Time	$V_{DS} = 300V$	t_r	—	33	—	
Turn off Delay Time	$I_D = 16.5A$	$t_{d(off)}$	—	80	—	
Fall Time	$R_G = 2.0\Omega, pw = 3\mu s$	t_f	—	23	—	
Diode Forward Voltage	$I_F = 23A, V_{GS} = 0V$	V_{SD}	—	1.0	1.5	V
	$I_F = 16.5A, V_{GS} = 0V$		—	0.87	—	
Diode Reverse Recovery Time	$I_F = 16.5A, di/dt = 100A/\mu sec$	t_{rr}	—	210	250	nsec
Peak Reverse Recovery Current		$I_{RM(rec)}$	—	tbd	—	A
Reverse Recovery Charge		Q_{rr}	—	1.3	—	μC
Safe Operating Area	$V_{DS} = 15.2V, 1 \text{ sec}, T_a = 25^\circ C$	SOA1	—		16.5	A
	$V_{DS} = 65V, 1 \text{ sec}, T_a = 25^\circ C$	SOA2	—		1.05	
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	4100	—	pF
Output Capacitance	$V_{DS} = 25V$	C_{oss}	—	400	—	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	120	—	

NOTES:

* Pulse Test: Pulse Width = 300μsec, Duty Cycle = 2%.

1/ For Ordering Information, Price, and Availability Contact Factory.

2/ Screening per MIL-PRF-19500.

3/ For Package Outlines / lead bending options / pinout configurations Contact Factory.

4/ Unless Otherwise Specified, All Electrical Characteristics @25°C.

Available Part Numbers:

Consult Factory

PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
TO-254 (M)	Pin 1	Pin 2	Pin 3
TO-254Z (Z)	Pin 1	Pin 2	Pin 3

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