Solid State Devices, Inc.
14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

SFF60N90E

60 AMP , 900 Volts, 0.22 Ω Avalanche Rated N-channel HiPower MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information [1/]

SFF 60 N 90 _E_ __

- **Drain Current**: 60 = 60A
- **Voltage**: 90 = 900V
- **Package** [3/ 4/]: 12 pin package
- **Screening** [2/]: __ = Not Screened; TX = TX Level; TXV = TXV Level; S = S Level

Features:

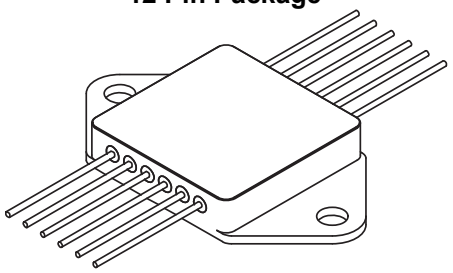
- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$ Q_G) figure of merit

Maximum Ratings [5/]		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	900	V
Gate – Source Voltage	continuous transient	V_{GS}	±20 ±30	V
Max. Continuous Drain Current (package limited)	@ T_C = 25ºC	I_{D1}	60	A
Max. Instantaneous Drain Current (Tj limited)	@ T_C = 25ºC	I_{D2}	150	A
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	60	A
Single and Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS} E_{AR}	4000 64	mJ
Total Power Dissipation	@ T_C = 25ºC	P_D	825	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	ºC
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.15	ºC/W

NOTES:

*Pulse Test: Pulse Width = 300µsec, Duty Cycle = 2%.
1/ For ordering information, price, and availability – contact factory.
2/ Screening based on MIL-PRF-19500. Screening flows available on request.
3/ For lead bending options / pinout configurations – contact factory.
4/ Maximum current limited by package configuration
5/ Unless otherwise specified, all electrical characteristics @25°C.

12 Pin Package



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.	**DATA SHEET #: FT0054A**	**DOC**

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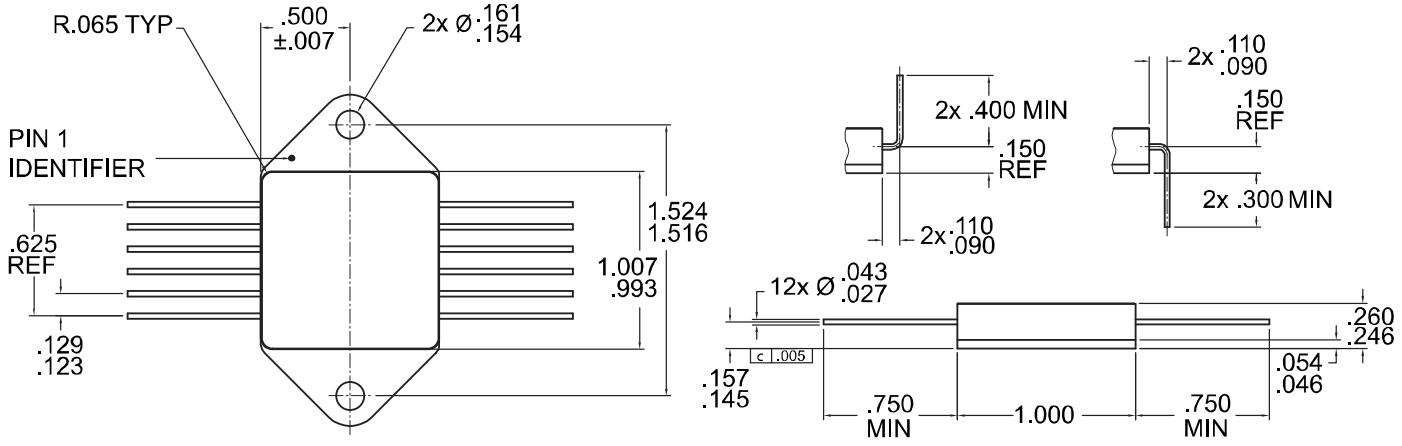
Electrical Characteristics[5/]		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 1 mA	BV_{DSS}	900	960	—	V
Drain to Source On State Resistance	V_{GS} = 10V, I_D = 18A, Tj= 25°C V_{GS} = 10V, I_D = 55A, Tj=25°C V_{GS} = 10V, I_D = 18A, Tj= 125°C	$R_{DS(on)}$	— — —	155 175 300	200 220 —	mΩ
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.0mA, Tj= 25°C V_{DS} = V_{GS}, I_D = 1.0mA, Tj= 125°C V_{DS} = V_{GS}, I_D = 1.0mA, Tj= -55°C	$V_{GS(th)}$	2.5 1.5 —	5.0 4.0 5.6	6.0 — 7.0	V
Gate to Source Leakage	V_{GS} = ±20V, Tj= 25°C V_{GS} = ±20V, Tj= 125°C	I_{GSS}	— —	10 30	±100 —	nA
Zero Gate Voltage Drain Current	V_{DS} = 720V, V_{GS} = 0V, T_j = 25°C V_{DS} = 900V, V_{GS} = 0V, T_j = 25°C V_{DS} = 720V, V_{GS} = 0V, T_j = 125°C	I_{DSS}	— —	0.5 10 350	- 100 2000	µA
Forward Transconductance	V_{DS} = 15V, I_D = 20A, T_j = 25°C	g_{fs}	-	45	—	Mho
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	V_{GS} = 10V V_{DS} = 500V I_D = 20A	Q_g Q_{gs} Q_{gd}	— — —	390 135 200	— — —	nC
Turn on Delay Time **Rise Time** **Turn off Delay Time** **Fall Time**	V_{GS} = 10V V_{DS} = 450V I_D = 10A	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	90 80 170 110	— — — —	nsec
Diode Forward Voltage	I_F = 60A, V_{GS} = 0V	V_{SD}	—	0.80	1.2	V
Diode Reverse Recovery Time **Reverse Recovery Charge**	I_F = 36A, di/dt = 100A/usec	t_{rr1} I_{rm1} Q_{rr1}	— — —	380 9 2000	— — —	nsec A nC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	V_{GS} = 0V V_{DS} = 25V f = 1 MHz	C_{iss} C_{oss} C_{rss}	— — —	9.2 1.4 380	— — —	nF nF pF

CASE OUTLINE: 12 Pin Package



Gate: pins 1, 12

Source: pins 2,3,4,9,10,11

Drain: pins 5,6,7,8