



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
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SFF26N100 Series

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF26N100

Screening ^{2/}
 — = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level
Lead Option ^{3/}
 — = Straight Leads
 DB = Down Bend
 UB = Up Bend
Package ^{3/ 4/}
 S2 = SMD2

N = TO-258
P = TO-259

**26 AMP , 1000 Volts, 175 mΩ
Avalanche Rated N-Channel
MOSFET**

Features:

- Rugged Poly-Si Gate
- Lowest ON-Resistance in the Industry
- Avalanche Rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, and S-Level Screening Available
- Improved ($R_{DS(ON)}$ OG) Figure of Merit

Maximum Ratings ^{5/}	Symbol	Value	Unit
Drain – Source Voltage	V_{DS}	1000	V
Gate – Source Voltage	V_{GS}	± 20 ± 30	V
Continuous Drain Current (T_{OP} limited) @ $T_C = 25^\circ C$	I_{D1}	26	A
Continuous Drain Current (T_{OP} limited) @ $T_C = 100^\circ C$	I_{D2}	16	A
Pulsed Drain Current (P_{width} / T_{OP} limited) @ $T_C = 25^\circ C$	I_{D3}	80	A
Single and Repetitive Avalanche Energy	E_{AS} E_{AR}	1200 2	mJ
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	300	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Thermal Resistance (Junction to Case)	$R_{\theta JC}$	0.42	$^\circ C/W$

NOTES:

*Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

^{1/} For ordering information, price, and availability - contact factory.

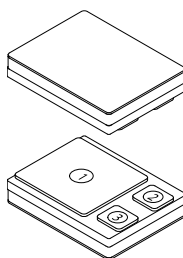
^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} For lead bending options / pinout configurations - contact factory.

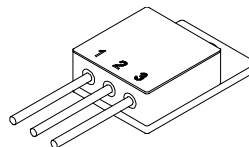
^{4/} Maximum current limited by package configuration

^{5/} Unless otherwise specified, all electrical characteristics @ $25^\circ C$.

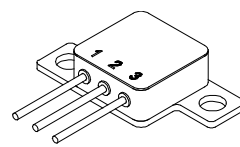
SMD2 (S2)



TO-258 (N)



TO-259 (P)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0062D

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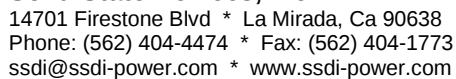
Series

Electrical Characteristics ^{5/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 0.5\text{ mA}$		BV_{DSS}	1000	1030	—	V
Drain to Source On State Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(on)}$	—	160	175	mΩ
	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 150^\circ\text{C}$		—	420	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 2\text{ mA}, T_J = 25^\circ\text{C}$	$V_{GS(th)}$	2.5	3.0	3.5	V
	$V_{DS} = V_{GS}, I_D = 2\text{ mA}, T_J = 125^\circ\text{C}$		1.5	2.0	—	
	$V_{DS} = V_{GS}, I_D = 2\text{ mA}, T_J = -55^\circ\text{C}$		—	4.0	4.5	
Gate to Source Leakage $V_{GS} = \pm 20\text{ V}, T_J = 25^\circ\text{C}$ $V_{GS} = \pm 20\text{ V}, T_J = 125^\circ\text{C}$		I_{GSS}	— —	1 10	± 200 —	nA
Zero Gate Voltage Drain Current	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	I_{DSS}	—	0.02	5	μA
	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$		—	10	300	μA
Total Gate Charge	$V_{GS} = 10\text{ V}$	Q_g	—	200	300	nC
Gate to Source Charge	$V_{DS} = 150\text{ V}$	Q_{gs}	—	25	50	
Gate to Drain Charge	$I_D = 20\text{ A}$	Q_{gd}	—	80	150	
Turn on Delay Time	$V_{GS} = 10\text{ V}$	$t_{d(on)}$	—	45	75	nsec
Rise Time	$V_{DS} = 150\text{ V}$	t_r	—	20	35	
Turn off Delay Time	$I_D = 20\text{ A}$	$t_{d(off)}$	—	150	250	
Fall Time		t_f	—	15	40	
Diode Forward Voltage $I_F = 20\text{ A}, V_{GS} = 0\text{ V}$		V_{SD}	—	0.9	1.1	V
Diode Reverse Recovery Time Reverse Recovery Charge	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	t_{rr1}	—	400	600	nsec
	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	I_{rm1}	—	27	—	A
	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	Q_{rr1}	—	5.5	—	μC
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	5000	—	pF
Output Capacitance	$V_{DS} = 50\text{ V}$	C_{oss}	—	600	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	—	—	

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