



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFC35N120

J

L

Screening^{2/}

— = Not Screened

TX = TX Level

TXV = TXV Level

S = S Level

Package^{3/}

J = TO-257

S.5 = SMD.5

G = Cerpack

SFC35N120

30 AMP, 1200 VOLTS, 96 mΩ
SiC Power MOSFET
Enhancement Mode N-Channel

Features:

- Fast Switching, Low Capacitance
- High Blocking Voltage, Low $R_{DS(ON)}$
- Easy to Parallel, Simple to Drive
- Resistant to Latch-Up
- Hermetically Sealed Power Packaging
- TX, TXV, S-Level Screening Available

Applications:

- High Voltage DC-DC Converters
- PFC Boost Converters
- Aerospace, Hi-Rel, Military

Maximum Ratings	Symbol	Value	Unit
Drain – Source Voltage	V_{DS}	1200	V
Gate – Source Voltage, Continuous	V_{GS}	+25, -10	V
Max. Continuous Drain Current @ $T_c = 25^\circ\text{C}$	I_{D1}	30 26	A
Max. Continuous Drain Current @ $T_c = 100^\circ\text{C}$	I_{D2}	18 16	A
Pulsed Drain Current, $t_p = 50 \mu\text{s}$ @ $T_c = 25^\circ\text{C}$	I_{D3}	90	A
Total Power Dissipation @ $T_c = 25^\circ\text{C}$	P_D	86 64	W
Operating & Storage Temperature	$T_{OP} \text{ \& } T_{STG}$	-55 to +150	$^\circ\text{C}$
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	1.45 1.95	$^\circ\text{C/W}$

NOTES:

*Pulse Test: Pulse Width = 300 μsec ,
Duty Cycle = 2%.

^{1/} For ordering information, price, and
availability - contact factory.

^{2/} Screening based on MIL-PRF-19500.
Screening flows available on request.

^{3/} Unless otherwise specified, all electrical
characteristics @25 $^\circ\text{C}$.

TO-257 (J)

SMD.5 (S.5)

Cerpack (G)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0079D

DOCX



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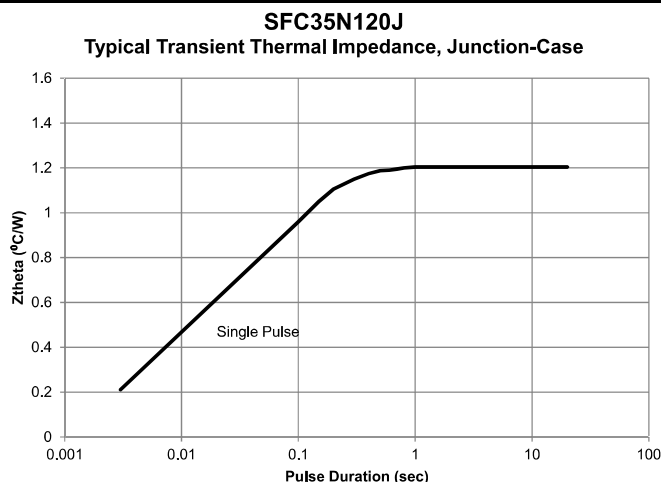
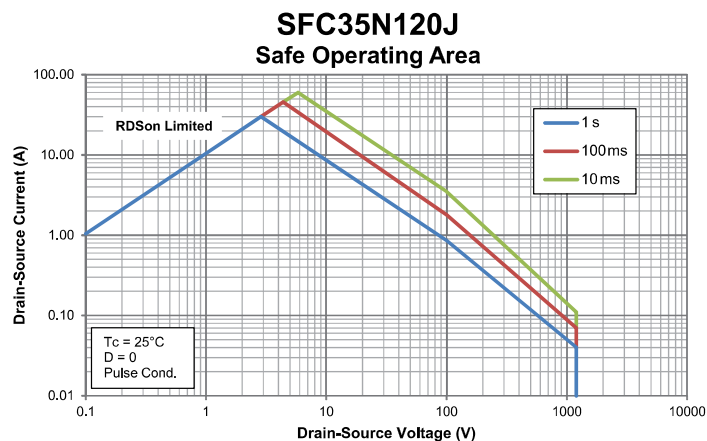
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Electrical Characteristics ^{3/}	Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 50\text{ }\mu\text{A}$	BV_{DSS}	1200	-	-	V
Drain to Source On State Resistance $V_{GS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 25^\circ\text{C}$ $V_{GS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 150^\circ\text{C}$	$R_{DS(on)}$	- -	80 150	96 190	m Ω
Gate Threshold Voltage $V_{DS} = 10\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$ $V_{DS} = 10\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	$V_{GS(th)}$	1.80 1.30	2.00 1.45	- -	V
Gate to Source Leakage $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$	I_{GSS}	-	90	500	nA
Zero Gate Voltage Drain Current $V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$ $V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$	I_{DSS}	- -	.01 .10	10 100	μA μA
Forward Transconductance $V_{DS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 25^\circ\text{C}$ $V_{DS} = 20\text{ V}, I_D = 20\text{ A}, T_J = 150^\circ\text{C}$	g_{fs}	- -	5.0 4.8	- -	Mho
Total Gate Charge $V_{GS} = -5\text{ V to } 20\text{ V}$	Q_g	-	46	65	nC
Gate to Source Charge $V_{DS} = 500\text{ V}$	Q_{gs}	-	8	-	nC
Gate to Drain Charge $I_D = 20\text{ A}$	Q_{gd}	-	18	-	nC
Turn On Delay Time	$t_{d(on)}$	-	18	40	ns
Rise Time $V_{DD} = 500\text{ V}, V_{GS} = 20\text{ V},$	t_r	-	20	45	
Turn Off Delay Time $I_D = 10\text{ A}, R_G = 0, t_P \geq 2\text{ }\mu\text{s}$	$t_{d(off)}$	-	24	50	
Fall Time	t_f	-	16	40	
Diode Forward Voltage $V_{GS} = -5\text{ V}, I_F = 10\text{ A}, T_J = 25^\circ\text{C}$ $V_{GS} = -2\text{ V}, I_F = 10\text{ A}, T_J = 150^\circ\text{C}$	V_{SD}	- -	4.3 3.5	6.5 -	V
Input Capacitance	C_{iss}	-	1050	1200	pF
Output Capacitance $V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	C_{oss}	-	220	300	
Reverse Transfer Capacitance	C_{rss}	-	10	20	
C_{oss} Stored Energy $V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}, f = 1\text{ MHz}$	E_{oss}	-	14	-	μJ
Internal Gate Resistance $V_{AC} = 25\text{ mV}, f = 1\text{ MHz}$	$R_{G(Int)}$	-	3.3	-	Ω



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PACKAGE OUTLINE:

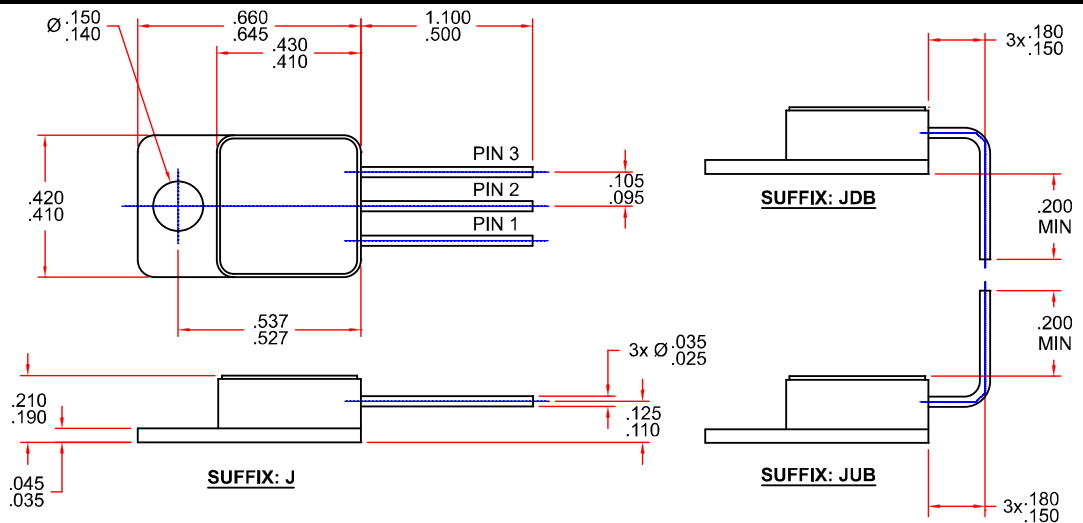
TO-257 (J)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



PACKAGE OUTLINE:

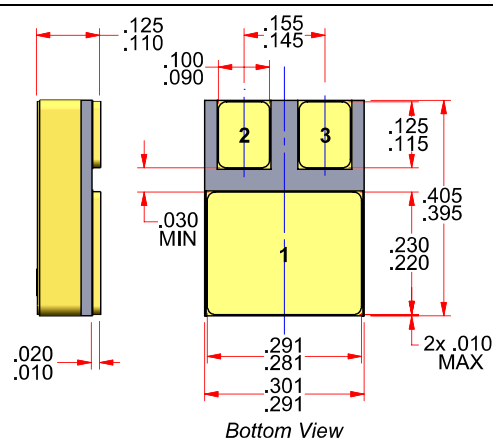
SMD.5 (S.5)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



PACKAGE OUTLINE:

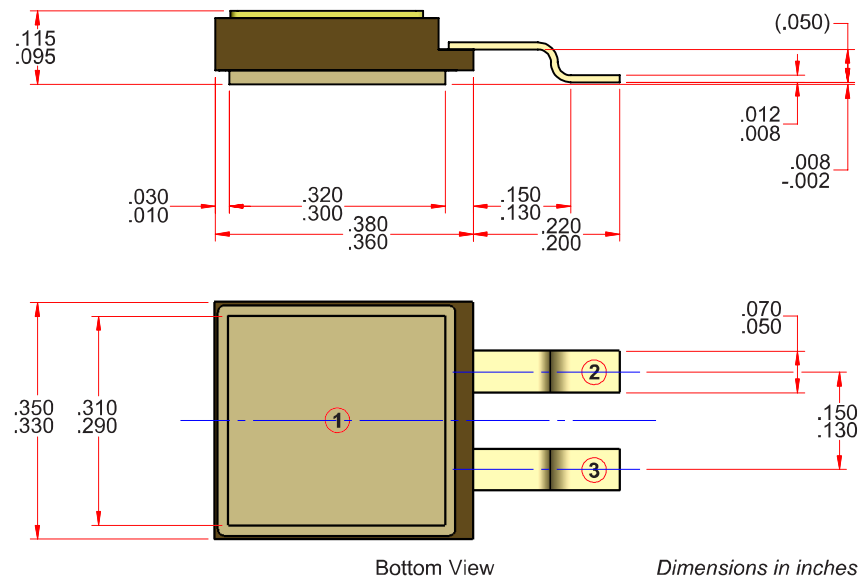
Cerpack (G)

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



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