NIKO-SEM

Dual N-Channel Enhancement Mode Field Effect Transistor

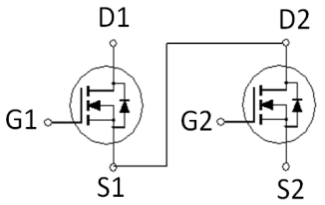
PK844DS

PDFN 5x6S

Halogen-Free & Lead-Free

PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
Q2	30V	1.4mΩ	85A
Q1	30V	5mΩ	53A

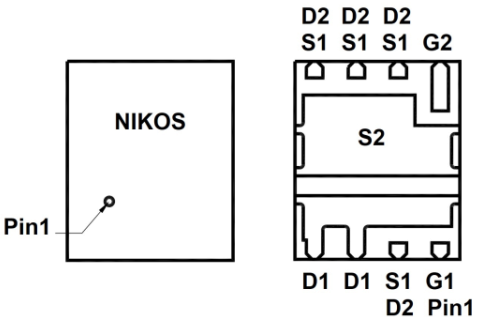


Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- 100% UIS and Rg Tested.

Applications

- Computing DC to DC converters.
- Communications DC to DC converters.
- General Purpose Point of load.



G: GATE
D: DRAIN
S: SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	Q2	Q1	UNITS
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±16	±20	V
Continuous Drain Current[3]	T_C=25 °C	I_D	85	53	A
	T_C=100 °C		85	33	
Pulsed Drain Current[1]		I_{DM}	255	120	
Continuous Drain Current	T_A=25 °C	I_D	39	18	
	T_A=70 °C		30	15	
Avalanche Current		I_{AS}	98	57	
Avalanche Energy	L=0.01mH	E_{AS}	48	16	mJ
Power Dissipation	T_C=25 °C	P_D	56	25	W
	T_C=100 °C		22	10	
Power Dissipation[4]	T_A=25 °C	P_D	3.6	3	W
	T_A=70 °C		2.3	1.9	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL		TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$	Q2		34	°C / W
			Q1		41	
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$	Q2		60	
			Q1		69	
Junction-to-Case	Steady-State	$R_{\theta JC}$	Q2		2.2	
			Q1		5	

[1]Pulse width limited by maximum junction temperature $T_{J(MAX)}$=150°C.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
[3]The maximum current rating is Package limited.
[4]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	Q2	30			V
			Q1	30			
Drain-Source Breakdown Voltage (transient)	$V_{(BR)DSSt}$	V_{GS} = 0V, $I_{D(aval)}$ = 12.6A, T_{case} = 25 °C , $t_{ransient}$ = 100ns	Q2	35			
			Q1	35			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	Q2	1.2	1.8	2.2	
			Q1	1.2	1.5	2.2	
Gate-Body Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±16V	Q2			±100	nA
		V_{DS}=0V, V_{GS}=±20V	Q1			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	Q2			1	μA
			Q1			1	
		V_{DS}=30V, V_{GS}=0V, T_J=55 °C	Q2			10	
			Q1			10	
Drain-Source On-State Resistance[5]	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=16A	Q2		1.5	1.9	mΩ
		V_{GS}=4.5V, I_D=13A	Q1		5.5	8	
		V_{GS}=10V, I_D=20A	Q2		0.91	1.4	
		V_{GS}=10V, I_D=13A	Q1		3.5	5	

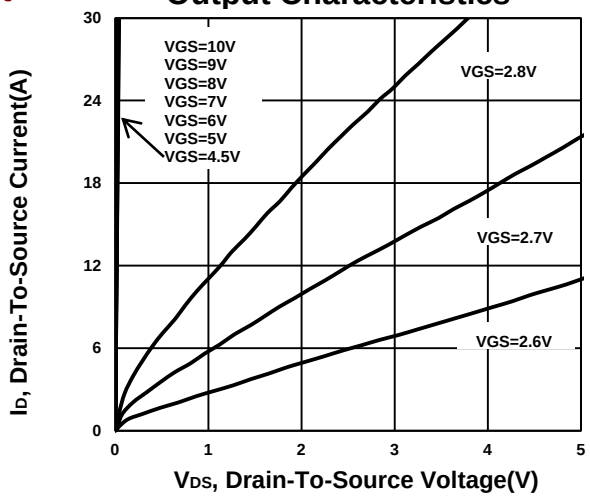
Forward Transconductance[5]	g_{fs}	V_{DS}=5V, I_D=20A	Q2		159		S
		V_{DS}=5V, I_D=13A	Q1		61		
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz	Q2		3845		pF
			Q1		1043		
Output Capacitance	C_{oss}		Q2		966		
			Q1		242		
Reverse Transfer Capacitance	C_{rss}		Q2		150		
			Q1		75		
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	Q2		0.9		Ω
			Q1		1.9		
Total Gate Charge[6]	Q_g VGS =10V	Q2 V_{DS}=15V, V_{GS}=10V, I_D=20A Q1 V_{DS}=15V, V_{GS}=10V, I_D=13A	Q2		65	91	nC
			Q1		19	27	
	Q_g VGS=4.5V		Q2		32	45	
			Q1		9.6	13.4	
Gate-Source Charge[6]	Q_{gs}		Q2		10		
			Q1		2.9		
Gate-Drain Charge[6]	Q_{gd}		Q2		11		
			Q1		4		
Turn-On Delay Time[6]	$t_{d(on)}$	Q2 V_{DS}=15V, I_D≅20A, V_{GS}=10V, R_{GEN}=6Ω Q1 V_{DS}=15V, I_D≅13A, V_{GS}=10V, R_{GEN}=6Ω	Q2		18		nS
			Q1		10		
Rise Time[6]	t_r		Q2		98		
			Q1		60		
Turn-Off Delay Time[6]	$t_{d(off)}$		Q2		75		
			Q1		28		
Fall Time[6]	t_f		Q2		107		
			Q1		70		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current	I_S		Q2			56	A
			Q1			20	
Forward Voltage[5]	V_{SD}	I_F=20A, V_{GS}=0V	Q2			1	V
		I_F=13A, V_{GS}=0V	Q1			1.2	
Reverse Recovery Time	t_{rr}	Q2 I_F=20A, dI_F/d =400A / μS Q1 I_F=13A, dI_F/dt=400A / μS	Q2		42		nS
			Q1		14		
Reverse Recovery Charge	Q_{rr}		Q2		85		nC
			Q1		15		

[5]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[6]Independent of operating temperature.

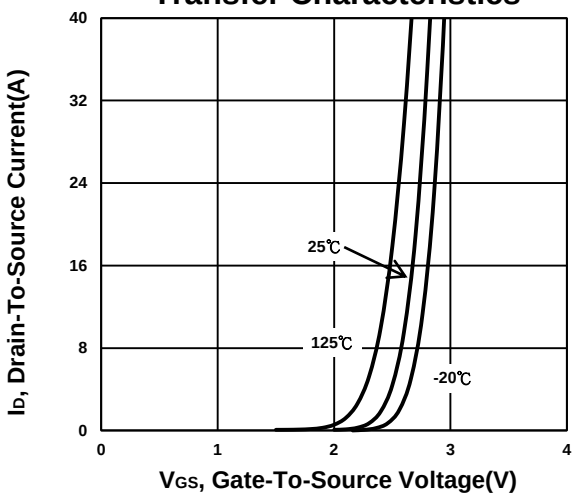
TYPICAL PERFORMANCE CHARACTERISTICS

Q2

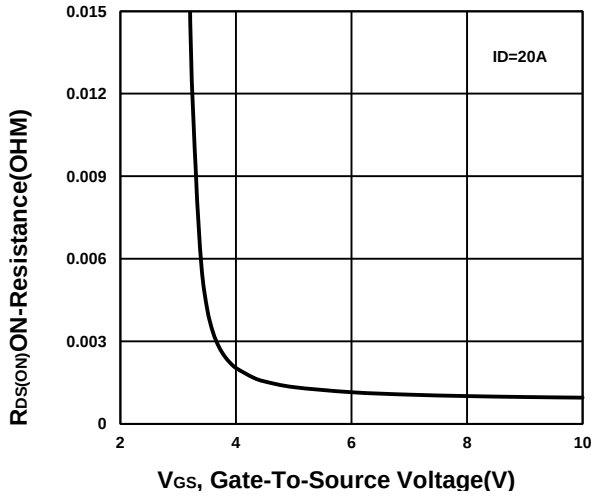
Output Characteristics



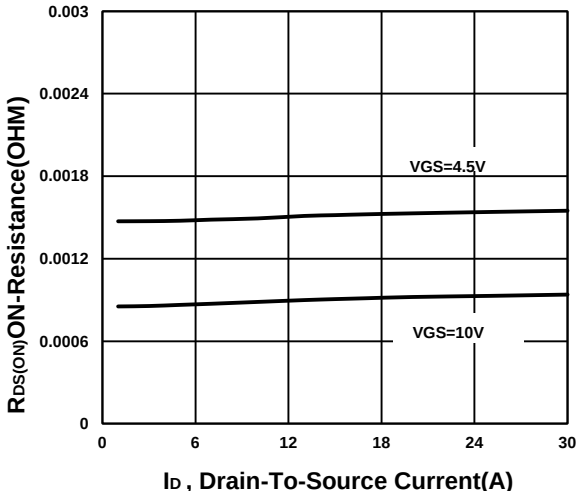
Transfer Characteristics



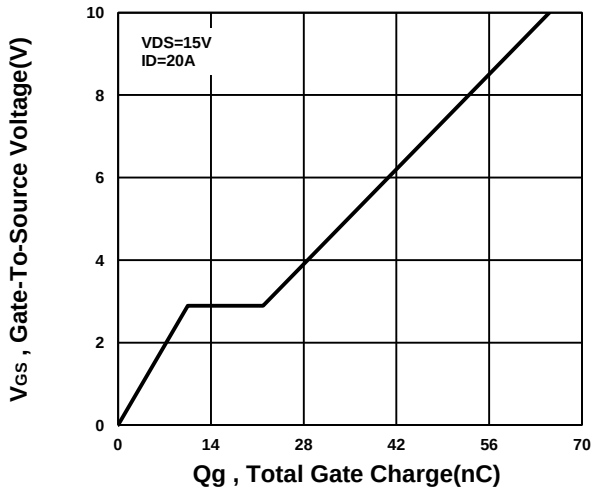
On-Resistance VS Gate-To-Source Voltage



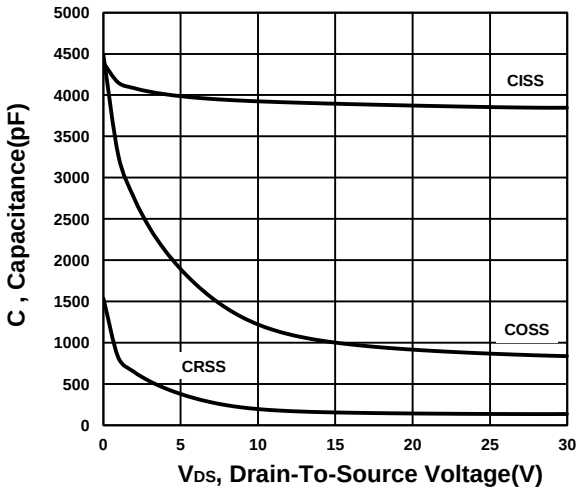
On-Resistance VS Drain Current



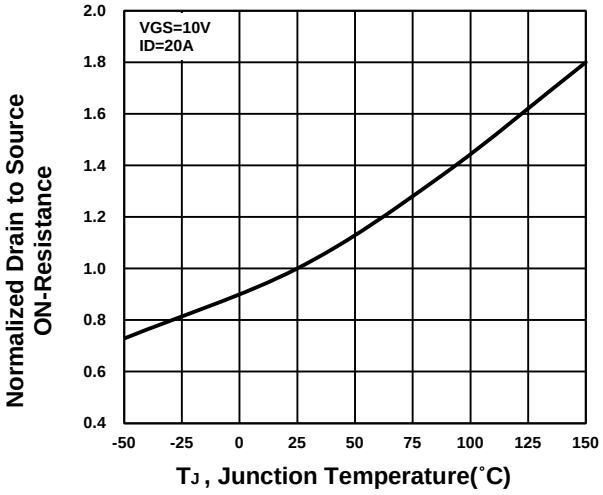
Gate charge Characteristics



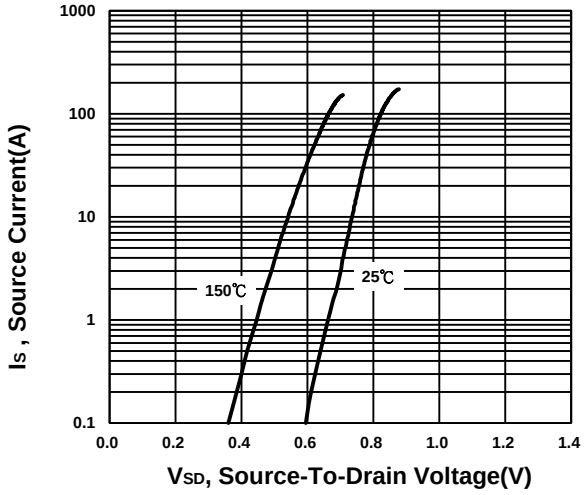
Capacitance Characteristic



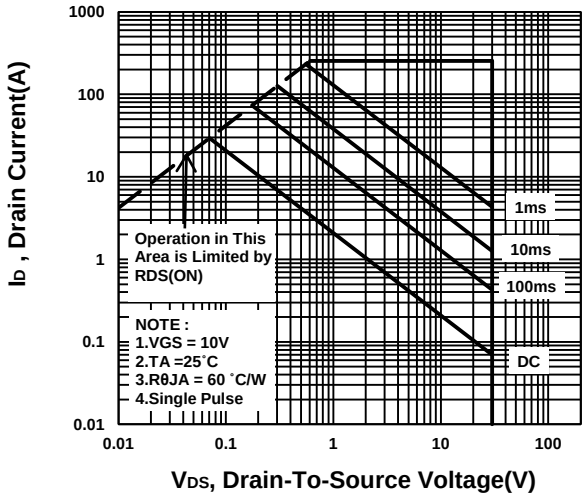
On-Resistance VS Temperature



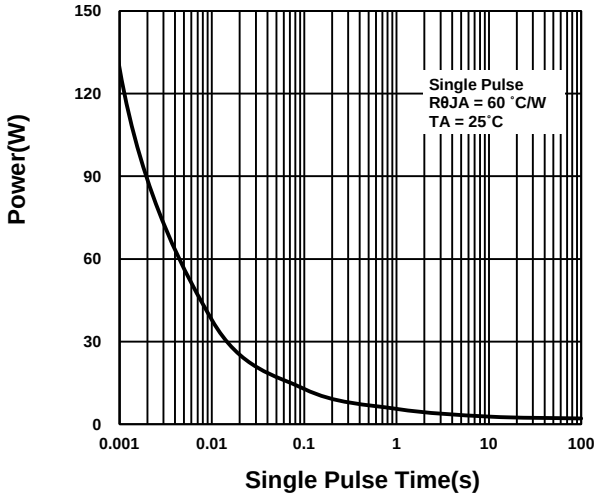
Source-Drain Diode Forward Voltage



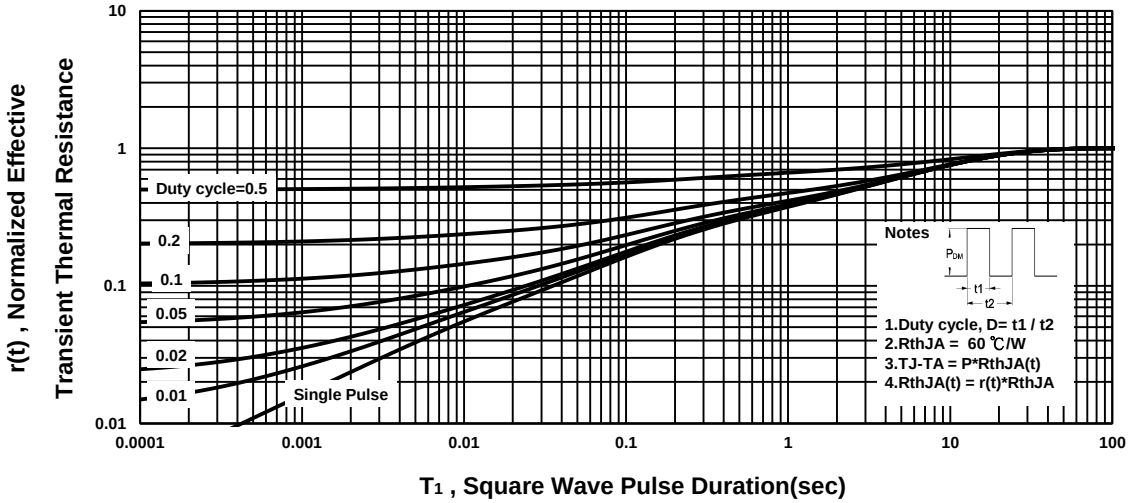
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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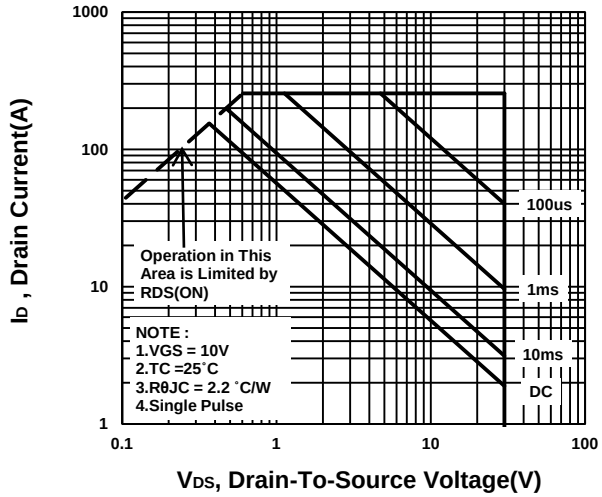

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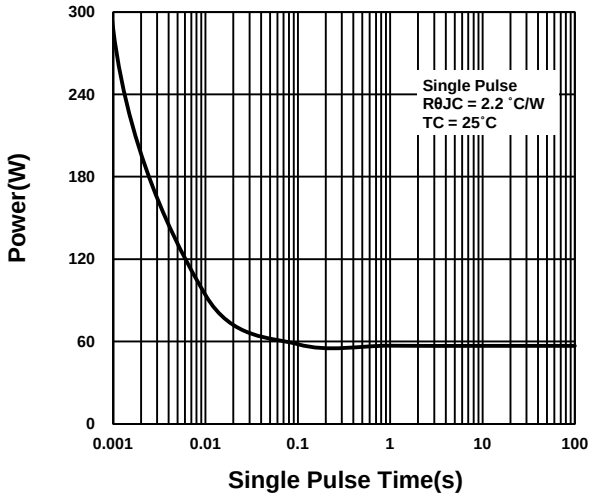
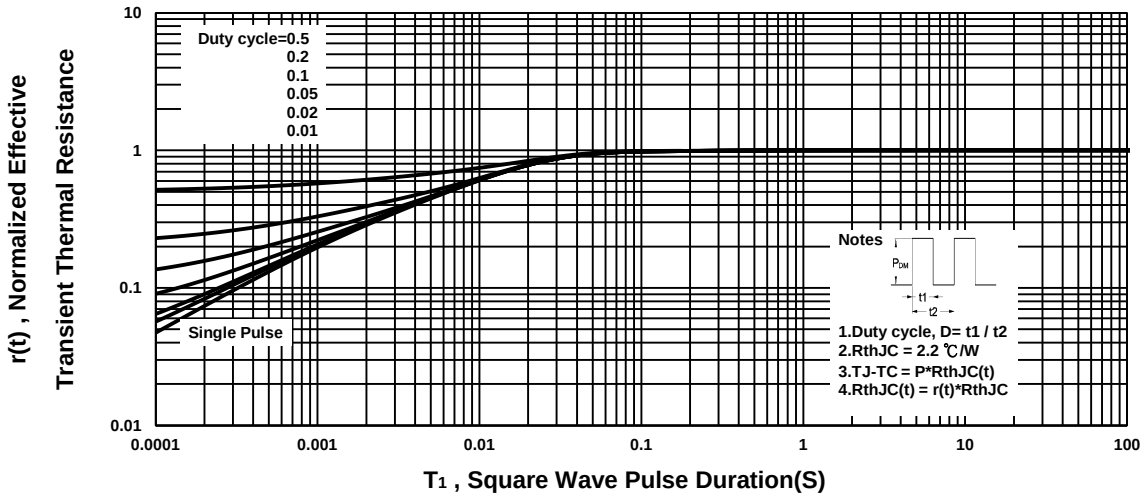
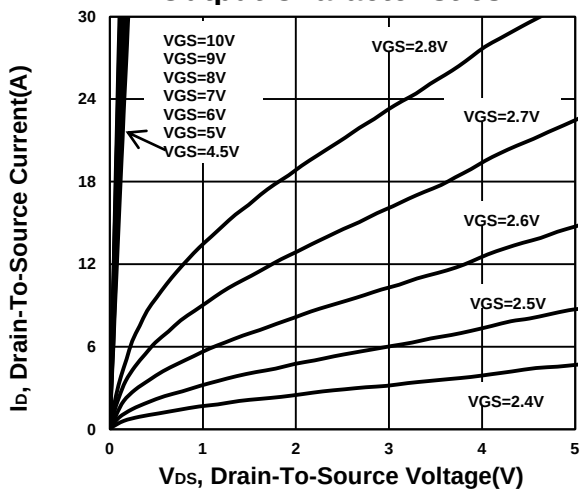


Transient Thermal Response Curve

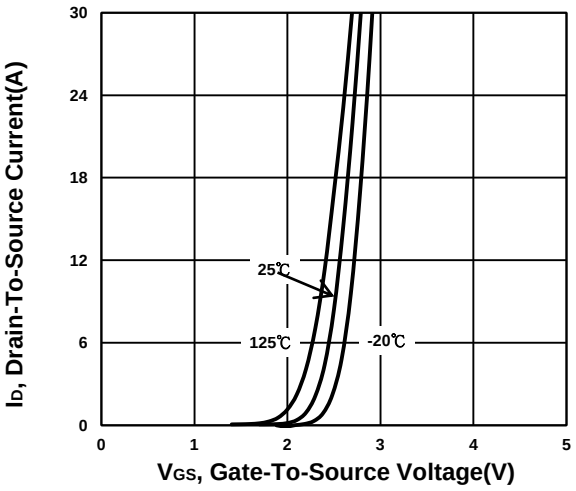


Q1

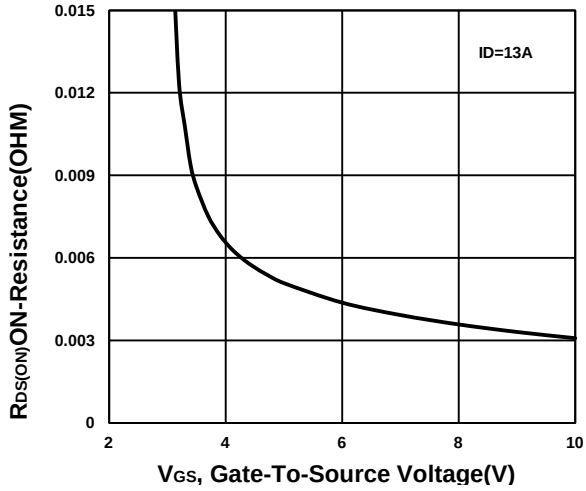
Output Characteristics



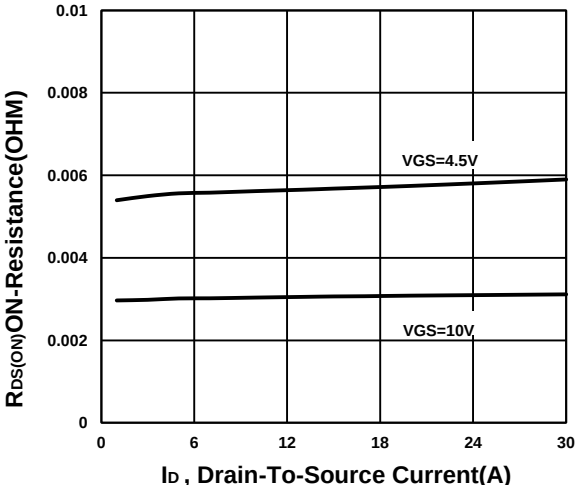
Transfer Characteristics



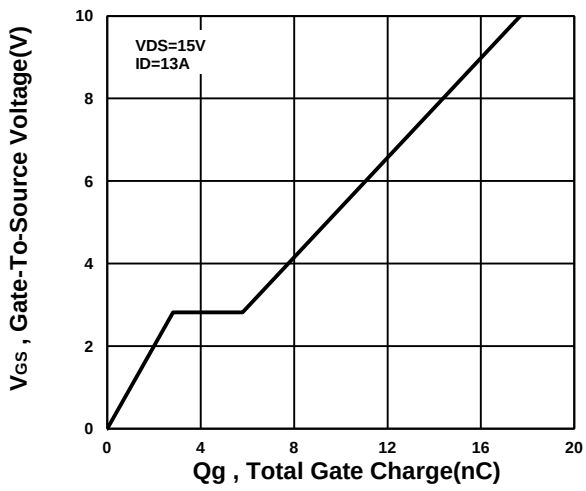
On-Resistance VS Gate-To-Source Voltage



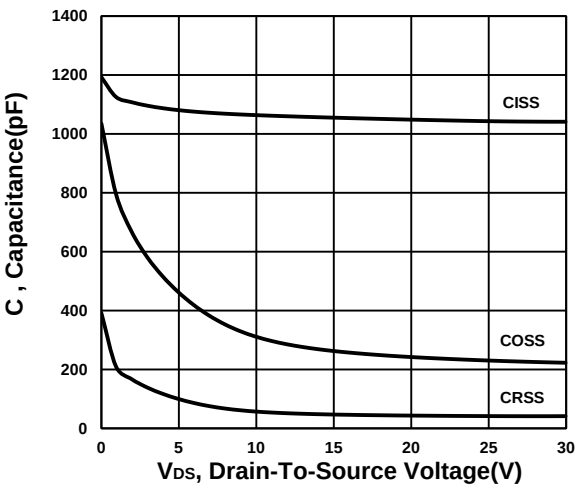
On-Resistance VS Drain Current



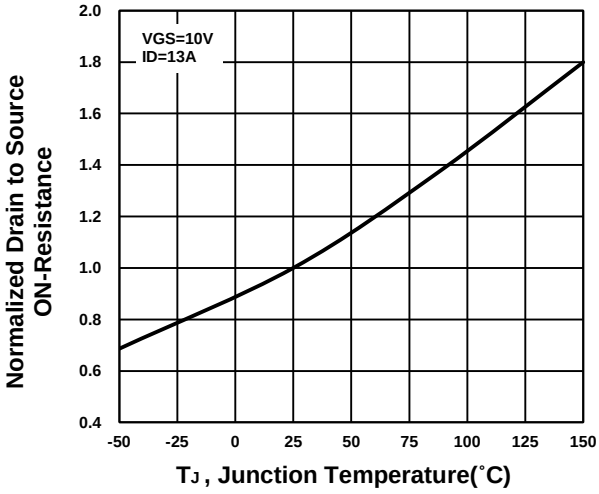
Gate charge Characteristics



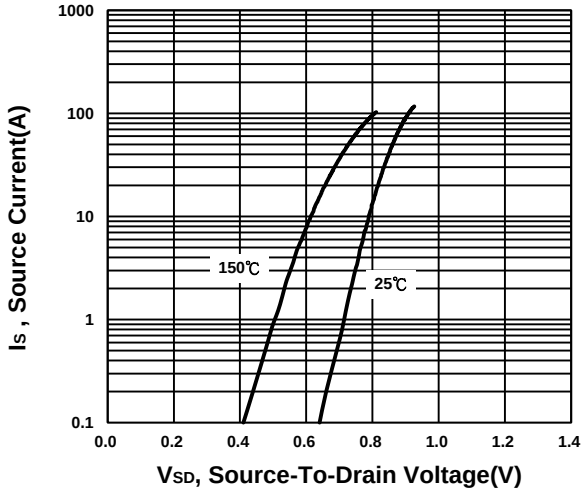
Capacitance Characteristic



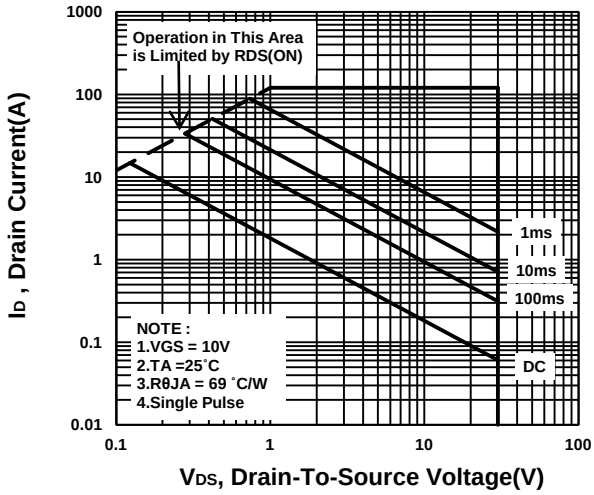
On-Resistance VS Temperature



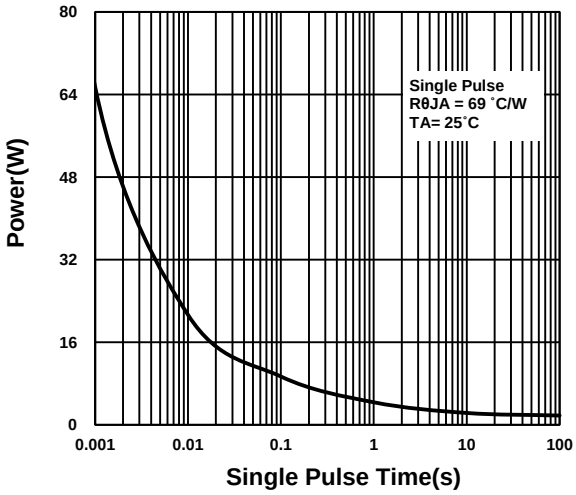
Source-Drain Diode Forward Voltage



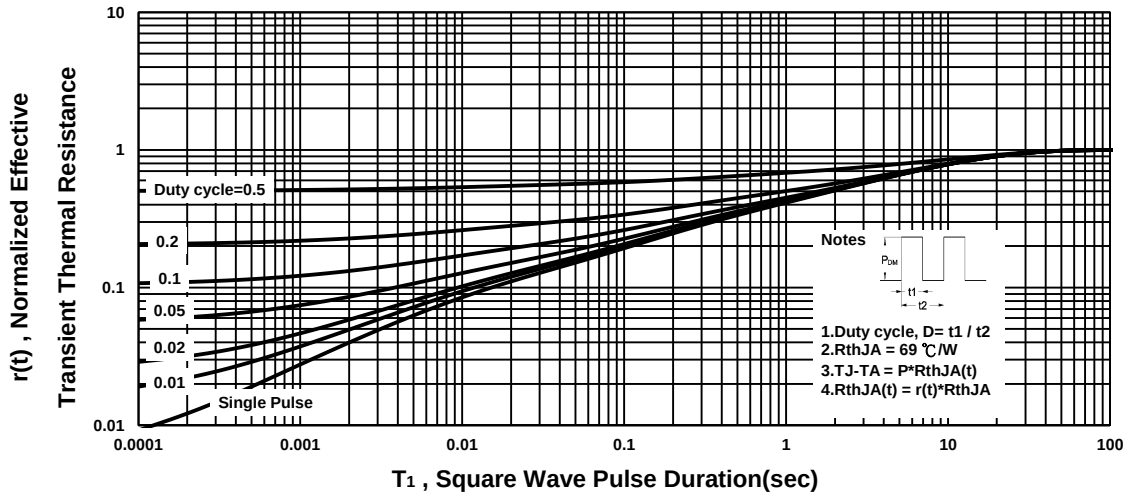
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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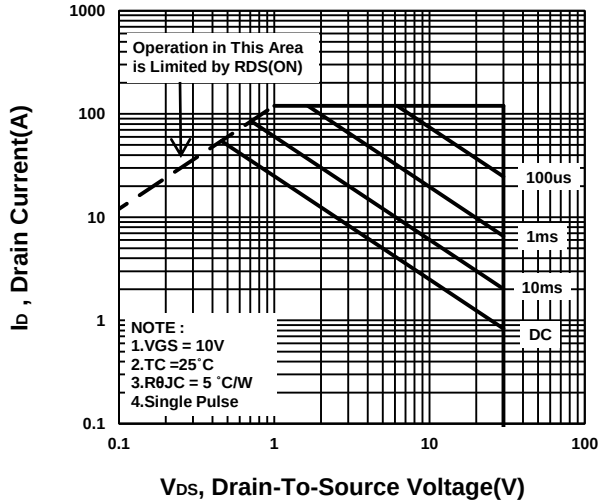

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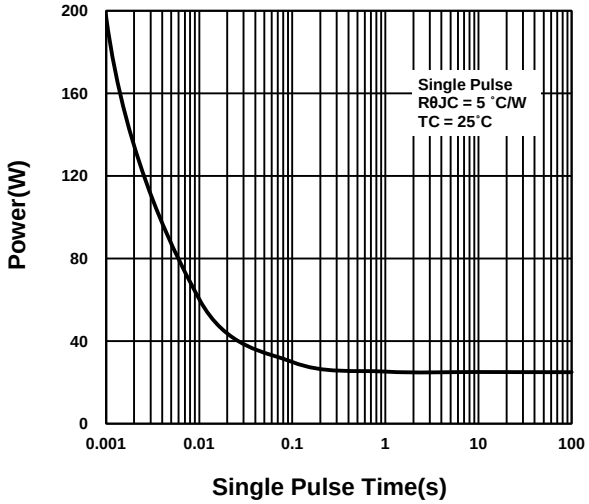

Transient Thermal Response Curve