NIKO-SEM

Dual N-Channel Enhancement Mode Field Effect Transistor

PK868HY

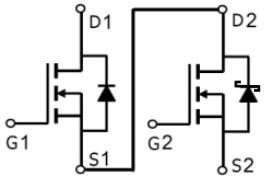
PDFN 5x6P

Halogen-Free & Lead-Free

RoHS Compliant

PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
Q2	30V	3mΩ	82A
Q1	30V	5mΩ	54A

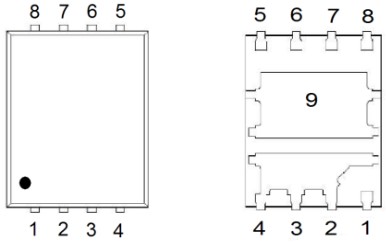


Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- Products Integrated Schottky Diode.
- 100% UIS and Rg Tested.

Applications

- Computing DC to DC converters.
- Communications DC to DC converters.
- General Purpose Point of load.



1 : G1
2,3,4 : D1
5,6,7 : S2
8 : G2
9 : S1/D2

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	Q2	Q1	UNITS
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	82	54	A
	T_C = 100 °C		51	34	
Pulsed Drain Current[1]		I_{DM}	150	95	
Continuous Drain Current	T_A = 25 °C	I_D	27	19	
	T_A = 70 °C		21	15	
Avalanche Current		I_{AS}	56	40	
Avalanche Energy	L = 0.03mH	E_{AS}	47	24	mJ
Power Dissipation	T_C = 25 °C	P_D	38	25	W
	T_C = 100 °C		15	10	
Power Dissipation[3]	T_A = 25 °C	P_D	4.2	3	W
	T_A = 70 °C		2.7	2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL		TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$	Q2		30	°C / W
			Q1		41	
	Steady-State	$R_{\theta JA}$	Q2		56	
			Q1		69	
Junction-to-Case		$R_{\theta JC}$	Q2		3.3	
		$R_{\theta JC}$	Q1		5	

[1]Pulse width limited by maximum junction temperature $T_{J(MAX)}$=150°C.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 1mA	Q2	30			V
		V_{GS} = 0V, I_D = 250μA	Q1	30			
Drain-Source Breakdown Voltage (transient)	$V_{(BR)DSSt}$	V_{GS} = 0V, $I_{D(aval)}$ = 12.6A T_{case} = 25 °C , $t_{ransient}$ = 100ns	Q2	34			
			Q1	34			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q2	1.3	1.7	2.3	
			Q1	1.3	1.9	2.3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q2			±100	nA
			Q1			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	Q2			0.5	mA
			Q1			1	μA
		V_{DS} = 20V, V_{GS} = 0V, T_J = 55 °C	Q2			5	mA
			Q1			10	μA
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} =4.5V, I_D = 16A	Q2		3.2	3.95	mΩ
		V_{GS} =4.5V, I_D = 13A	Q1		7.2	9.5	
		V_{GS} = 10V, I_D = 20A	Q2		2.4	3	
		V_{GS} = 10V, I_D = 13A	Q1		4.2	5	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A	Q2		100		S
		V_{DS} = 5V, I_D = 13A	Q1		50		

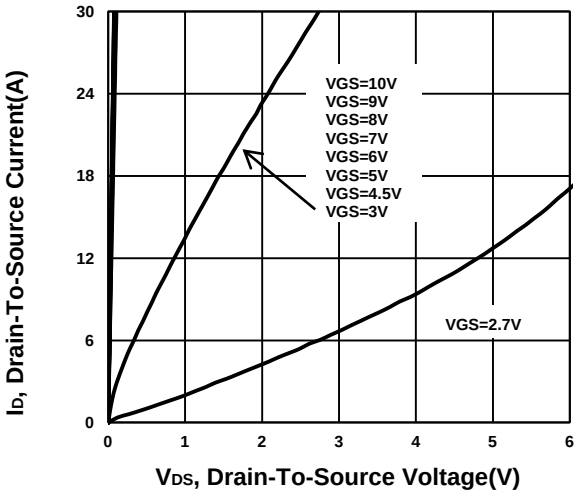
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	Q2		1850		pF
			Q1		1097		
Output Capacitance	C_{oss}		Q2		419		
			Q1		239		
Reverse Transfer Capacitance	C_{rss}		Q2		252		
			Q1		72		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	Q2		1.7		Ω
			Q1		1.7		
Total Gate Charge[2]	Q_g VGS = 10V	Q2 V_{DS} = 15V , V_{GS} = 10V, I_D = 20A Q1 V_{DS} = 15V , V_{GS} = 10V, I_D = 13A	Q2		38		nC
			Q1		20		
	Q_g VGS = 4.5V		Q2		20		
			Q1		10		
Gate-Source Charge[2]	Q_{gs}		Q2		5.3		
			Q1		3.3		
Gate-Drain Charge[2]	Q_{gd}		Q2		9.2		
			Q1		4.1		
Turn-On Delay Time[2]	$t_{d(on)}$	Q2 V_{DS} = 15V , $I_D \cong$ 20A, V_{GS} = 10V, R_{GEN} =6Ω Q1 V_{DS} = 15V , $I_D \cong$ 13A, V_{GS} = 10V, R_{GEN} =6Ω	Q2		10		nS
			Q1		8.6		
Rise Time[2]	t_r		Q2		89		
			Q1		69		
Turn-Off Delay Time[2]	$t_{d(off)}$		Q2		52		
			Q1		26		
Fall Time[2]	t_f		Q2		92		
			Q1		67		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current	I_S		Q2			38	A
			Q1			21	
Forward Voltage[1]	V_{SD}	I_F = 20A, V_{GS} = 0V	Q2			1	V
		I_F = 13A, V_{GS} = 0V	Q1			1.2	
Reverse Recovery Time	t_{rr}	Q2 I_F = 20A, dI_F/dt = 400A / µS Q1 I_F = 13A, dI_F/dt = 400A / µS	Q2		23		nS
			Q1		38		
Reverse Recovery Charge	Q_{rr}		Q2		23		nC
			Q1		30		

[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

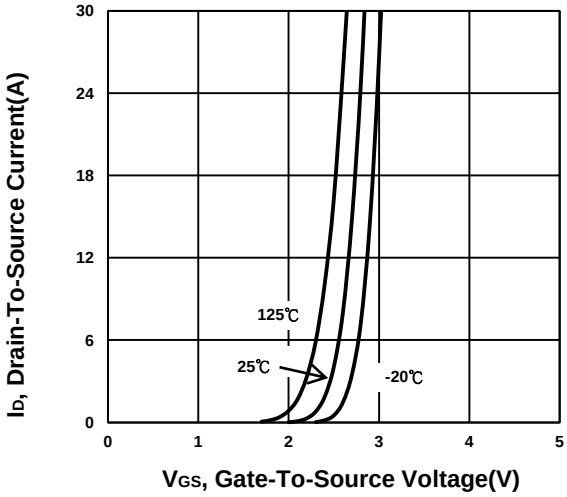
TYPICAL PERFORMANCE CHARACTERISTICS

Q2

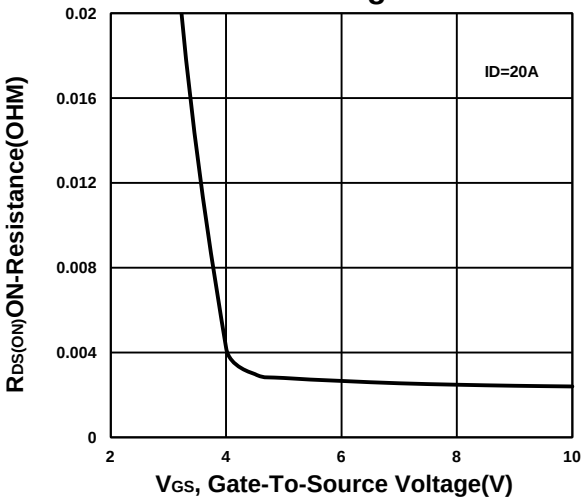
Output Characteristics



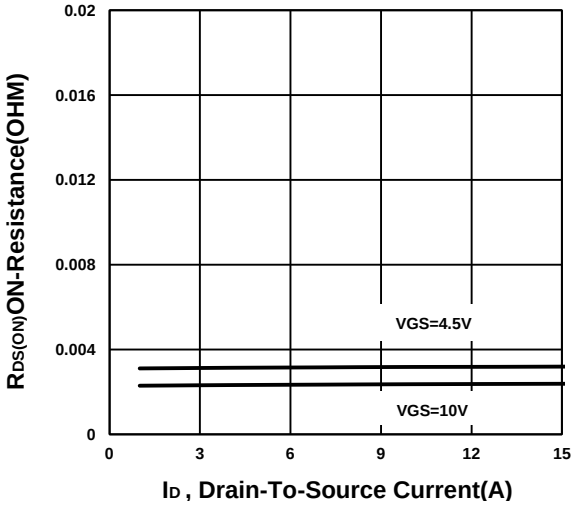
Transfer Characteristics



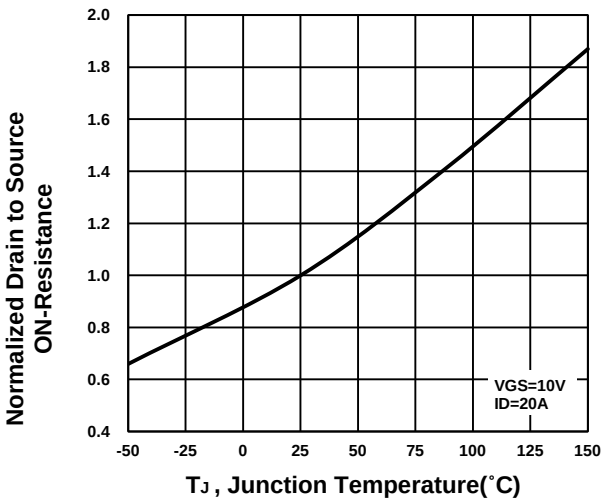
On-Resistance VS Gate-To-Source Voltage



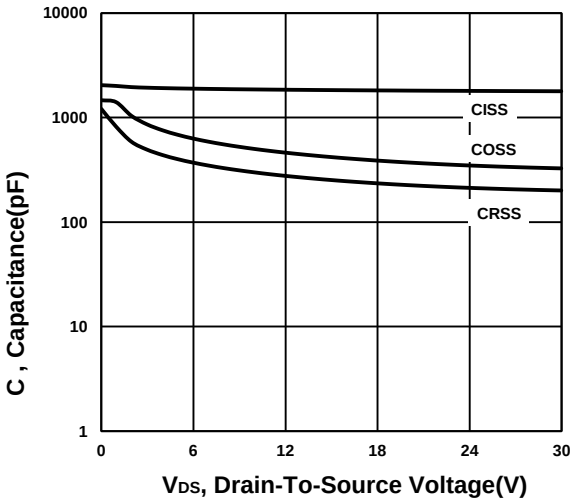
On-Resistance VS Drain Current



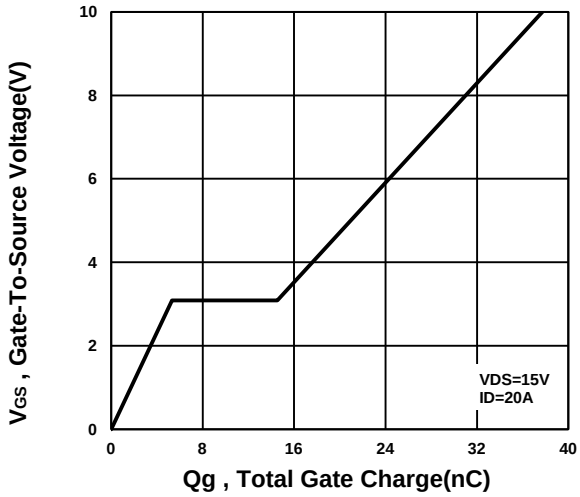
On-Resistance VS Temperature



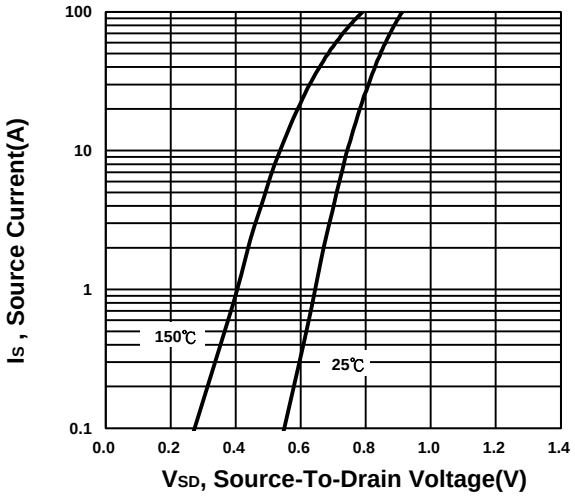
Capacitance Characteristic



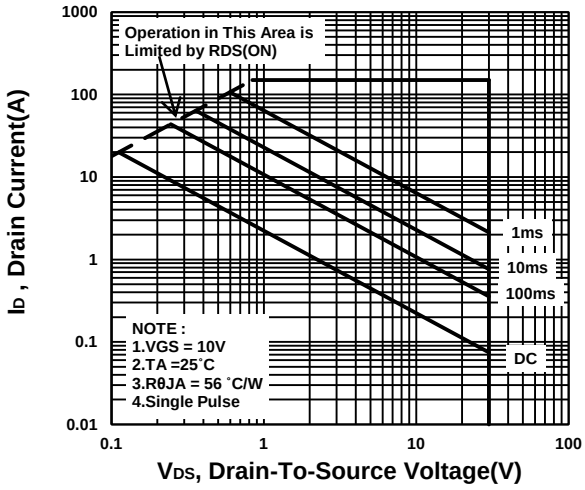
Gate charge Characteristics



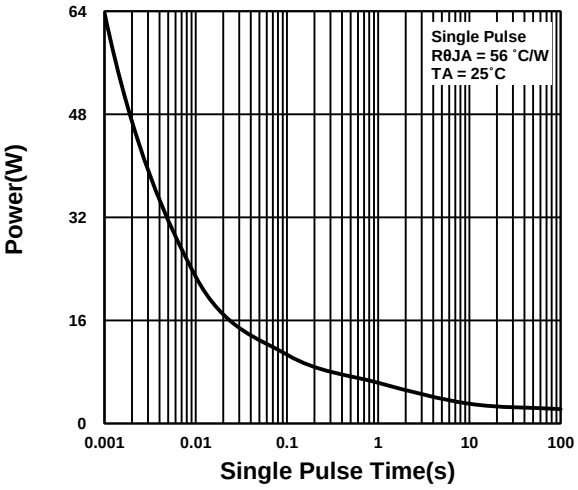
Source-Drain Diode Forward Voltage



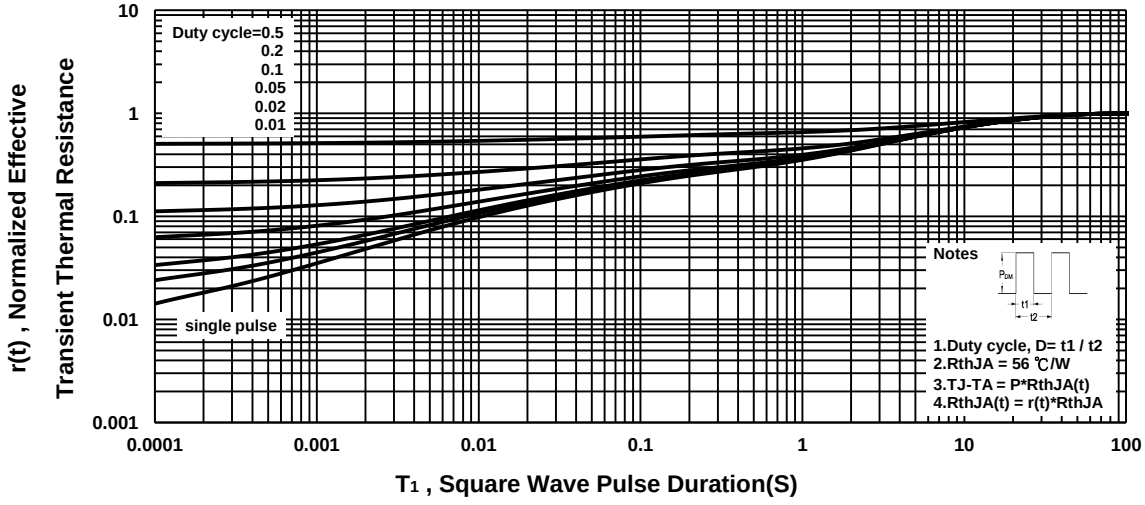
Safe Operating Area



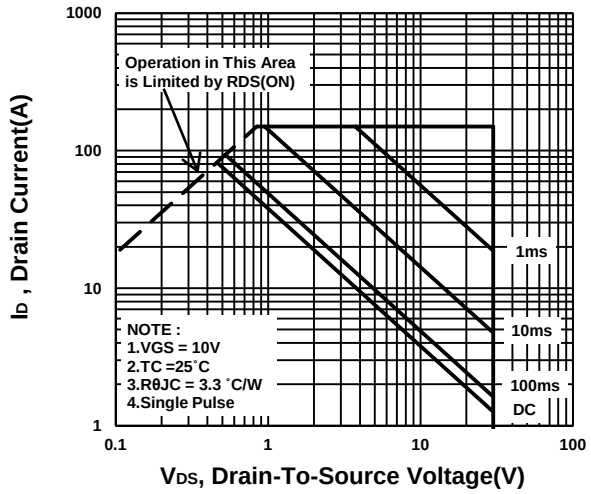
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Safe Operating Area



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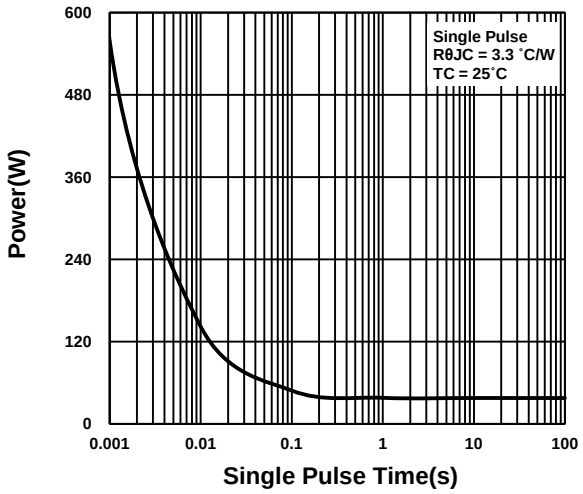

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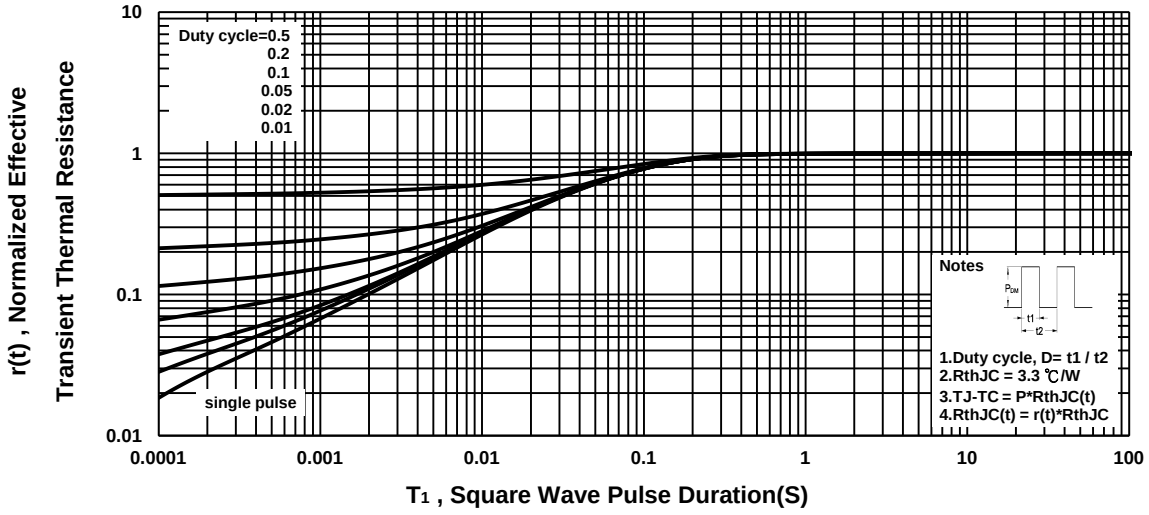
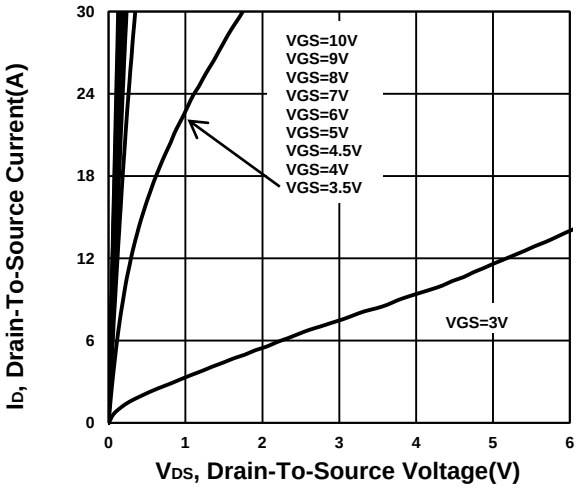
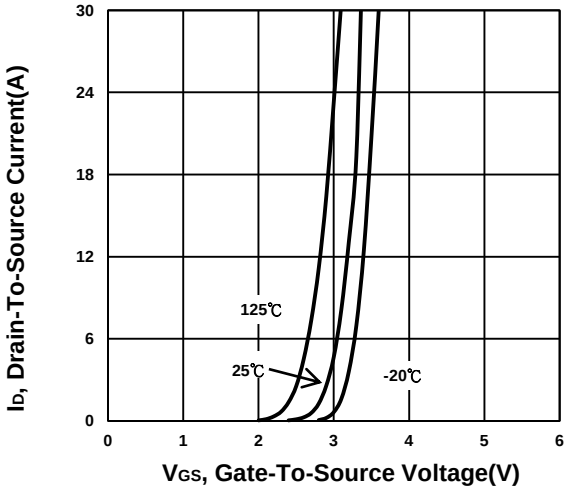


Q1

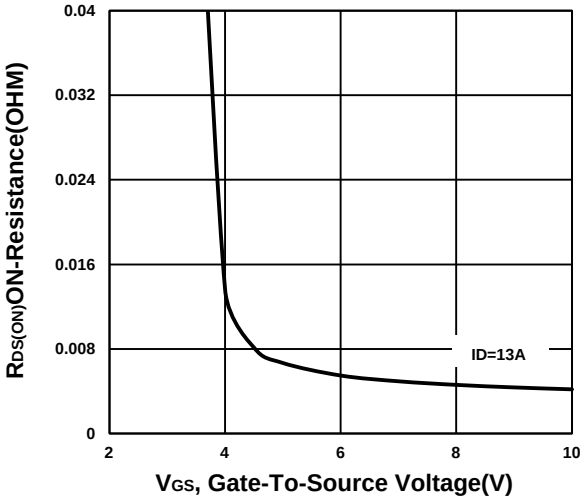
Output Characteristics



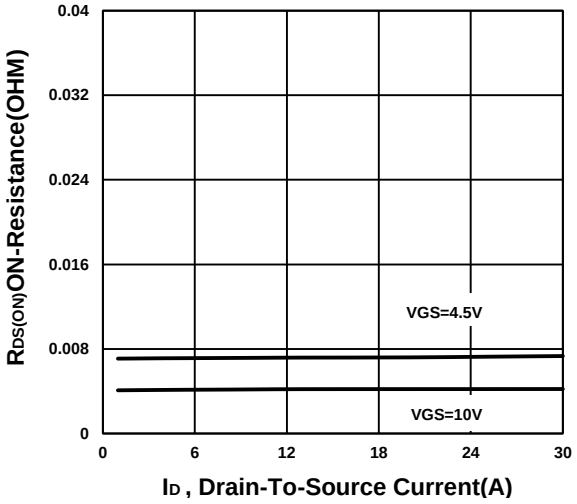
Transfer Characteristics



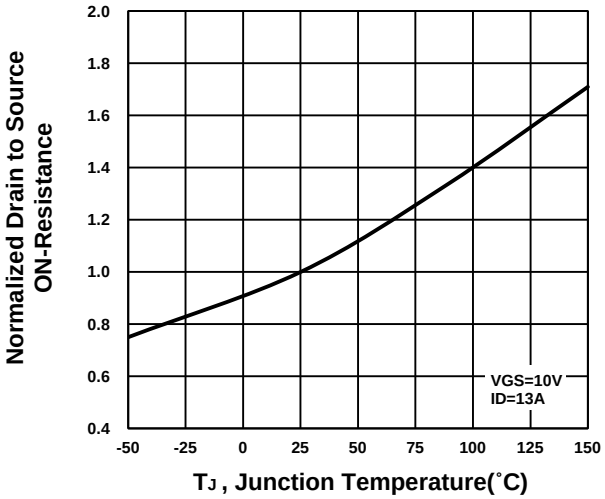
On-Resistance VS Gate-To-Source Voltage



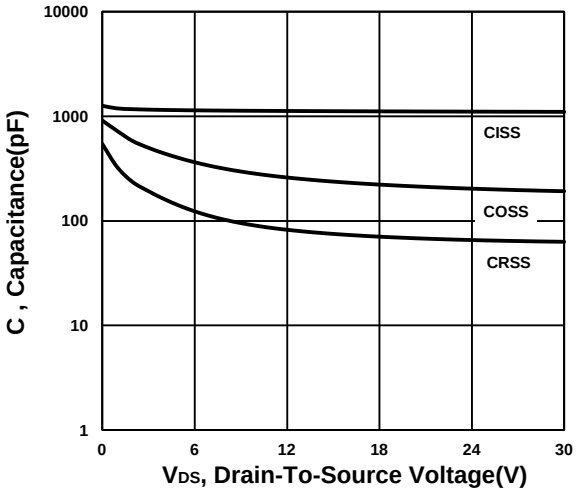
On-Resistance VS Drain Current



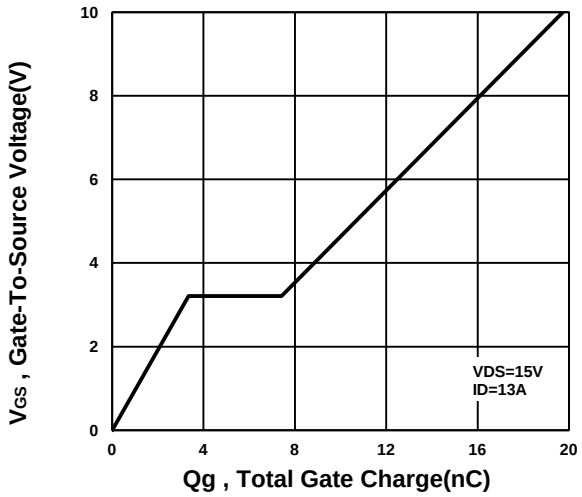
On-Resistance VS Temperature



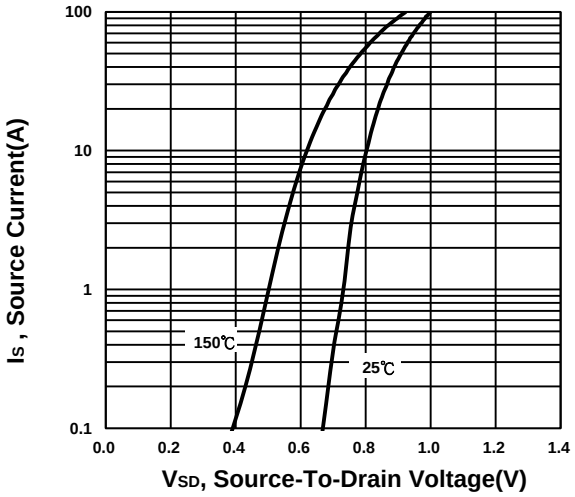
Capacitance Characteristic



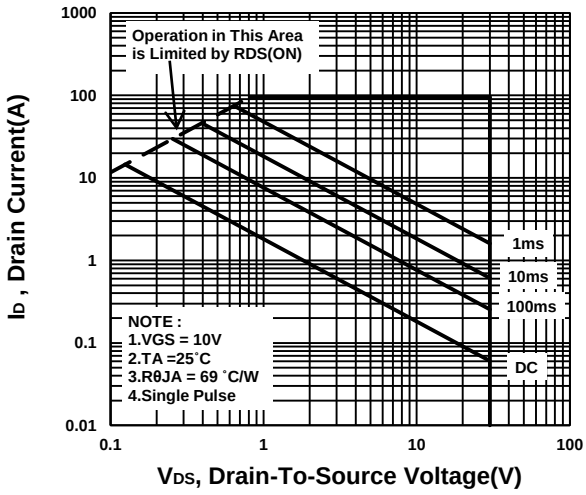
Gate charge Characteristics



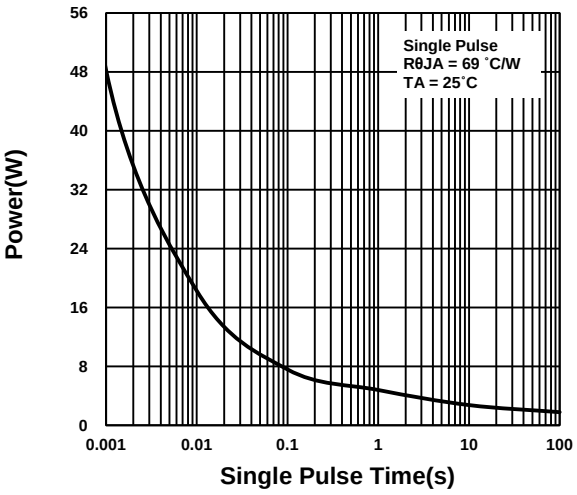
Source-Drain Diode Forward Voltage



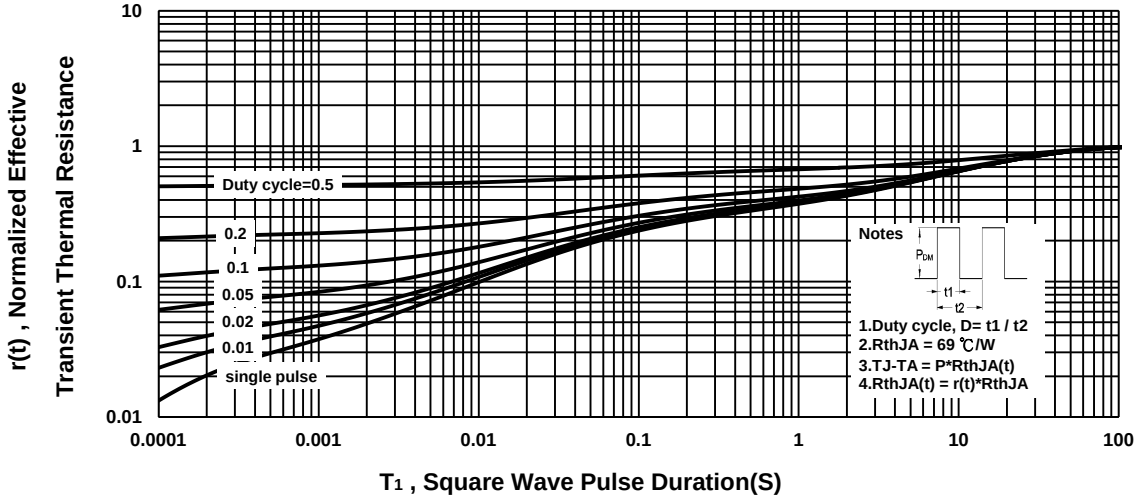
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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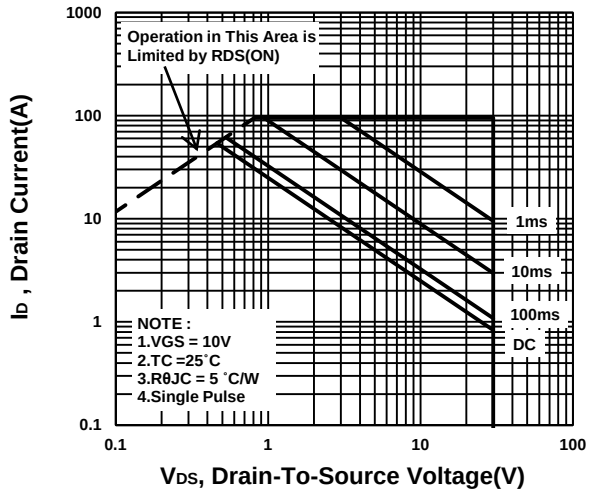

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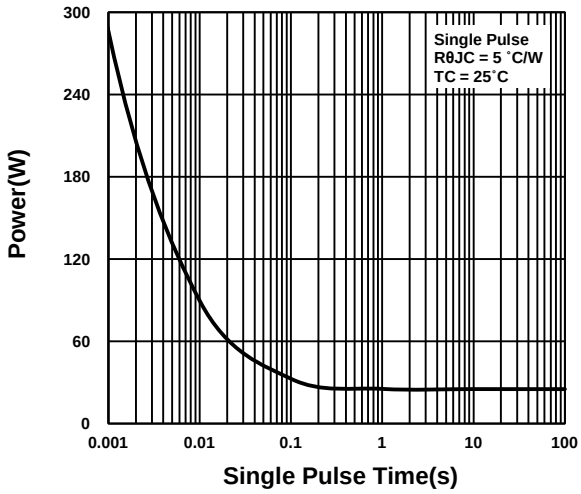

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