P-Channel Logic Level Enhancement Mode Field Effect Transistor

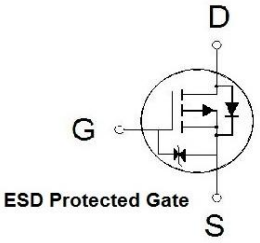
PECH1EU

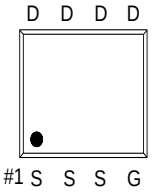
PDFN 3.3x3.3S

Halogen-free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	6.1mΩ	-50A





G. GATE
D. DRAIN
S. SOURCE

Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- 100% UIS and Rg Tested.
- Products Integrated ESD diode with ESD Protected.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current[4]	T_C = 25 °C	I_D	-50	A
	T_C = 100 °C		-46	
	T_A = 25 °C		-17	
	T_A = 70 °C		-13	
Pulsed Drain Current[1]		I_{DM}	-187	
Avalanche Current		I_{AS}	-54	
Avalanche Energy	L = 0.1mH	E_{AS}	145	mJ
Power Dissipation[3]	T_C = 25 °C	P_D	57	W
	T_C = 100 °C		23	
	T_A = 25 °C		3.1	
	T_A = 70 °C		2	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$		40	°C / W
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$		58	
Junction-to-Case	Steady-State	$R_{\theta JC}$		2.2	

[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.
[4]The maximum current rating is Package limited.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

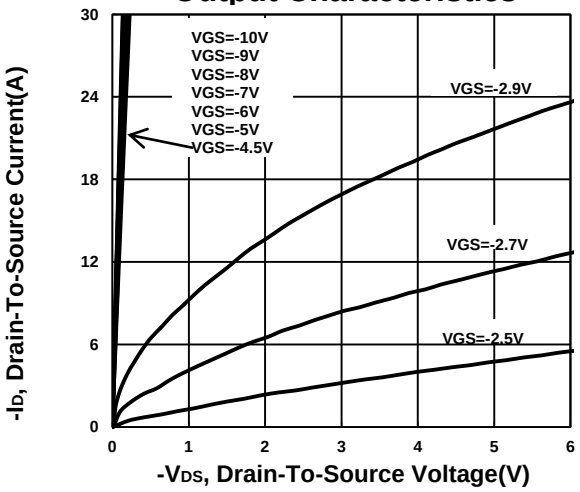
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.3	-1.7	-2.3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±25V			±10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	μA
		V_{DS} = -30V, V_{GS} = 0V, T_J = 55 °C			-10	
Drain-Source On-State Resistance[5]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -12A		4.7	6.1	mΩ
		V_{GS} = -4.5V, I_D = -12A		7.6	11	
Forward Transconductance[5]	g_{fs}	V_{DS} = -5V, I_D = -12A		45		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		3265		pF
Output Capacitance	C_{oss}			511		
Reverse Transfer Capacitance	C_{rss}			397		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		4.3		Ω
Total Gate Charge[6]	$Q_{g(VGS=-10V)}$	V_{DS} = -15V , I_D = -12A		67		nC
	$Q_{g(VGS=-4.5V)}$			33		
Gate-Source Charge[6]	Q_{gs}			9		
Gate-Drain Charge[6]	Q_{gd}			14		

Turn-On Delay Time[6]	$t_{d(on)}$	V_{DD} = -15V $I_D \cong$ -8.8A, V_{GS} = -10V, R_{GEN} = 2.6Ω		12		nS
Rise Time[6]	t_r			47		
Turn-Off Delay Time[6]	$t_{d(off)}$			87		
Fall Time[6]	t_f			78		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-48	A
Forward Voltage[5]	V_{SD}	I_F = -12A, V_{GS} = 0V			-1.3	V
Reverse Recovery Time	t_{rr}	I_F = -12A, dI/dt = 100A/μs		14		nS
Reverse Recovery Charge	Q_{rr}			2		nC

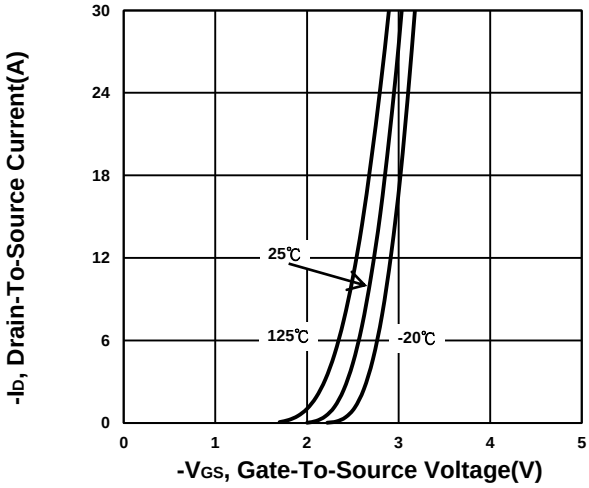
[5]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[6]Independent of operating temperature.

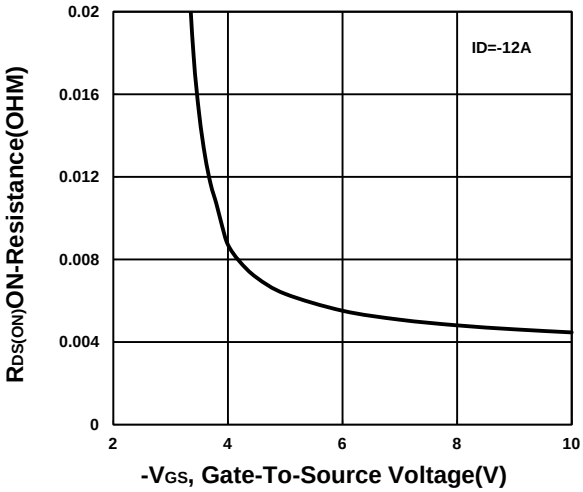
Output Characteristics



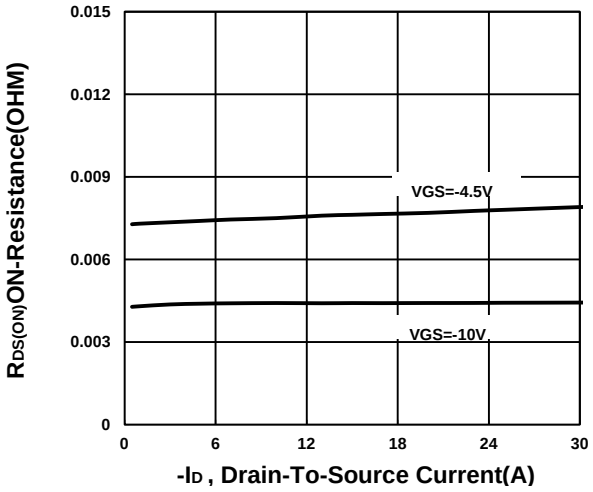
Transfer Characteristics



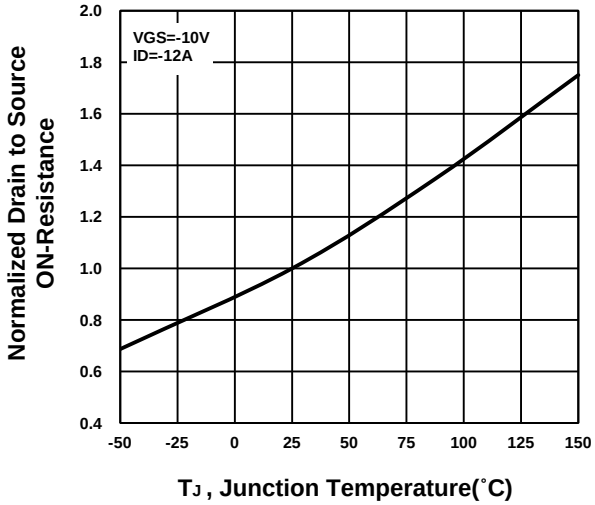
On-Resistance VS Gate-To-Source Voltage



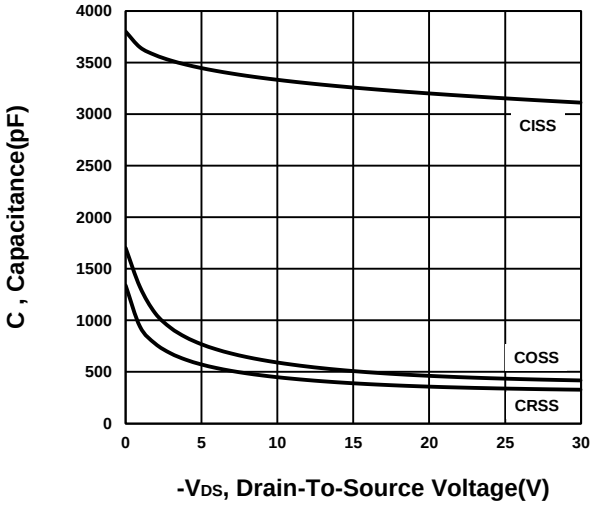
On-Resistance VS Drain Current



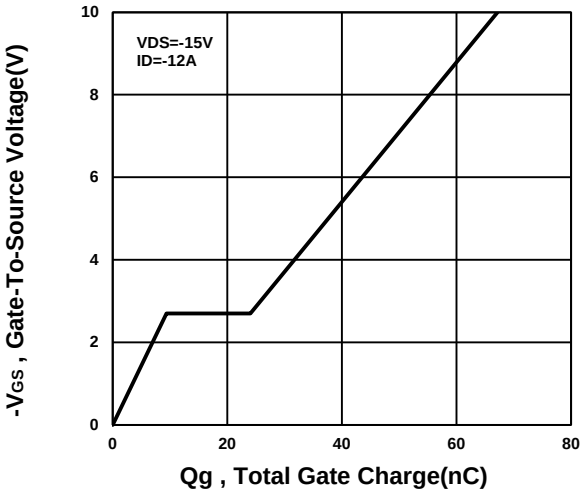
On-Resistance VS Temperature



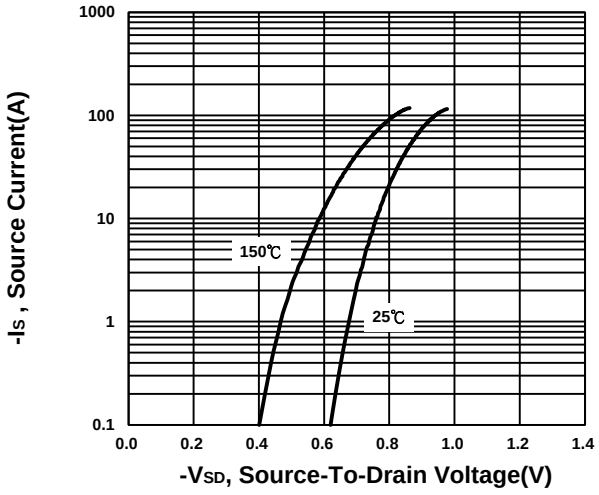
Capacitance Characteristic



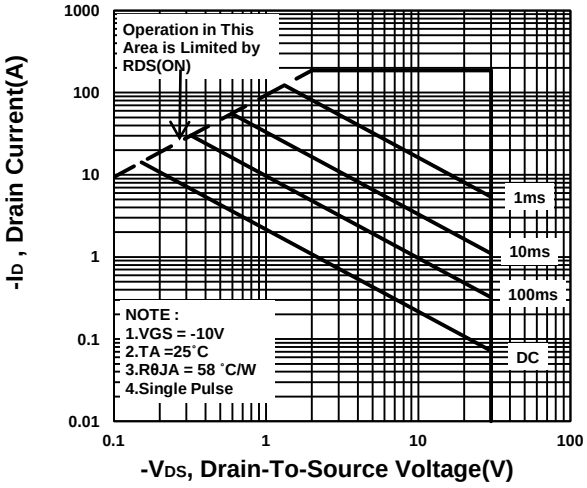
Gate charge Characteristics



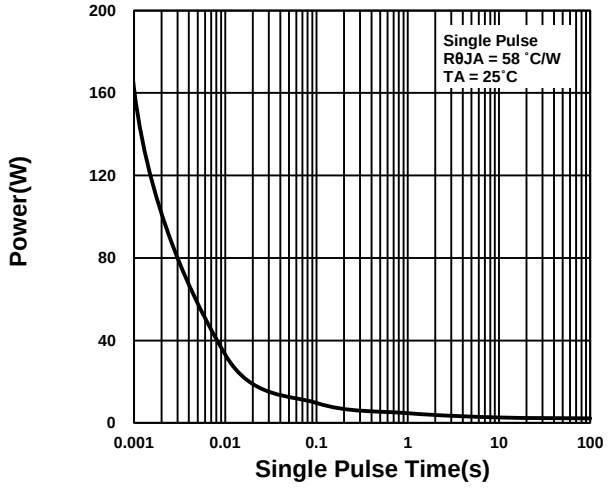
Source-Drain Diode Forward Voltage



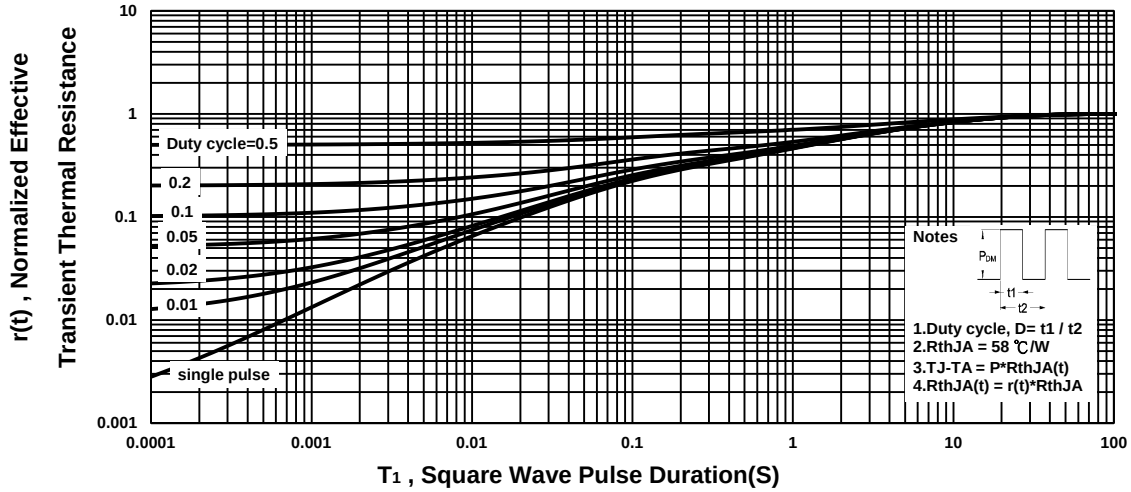
Safe Operating Area



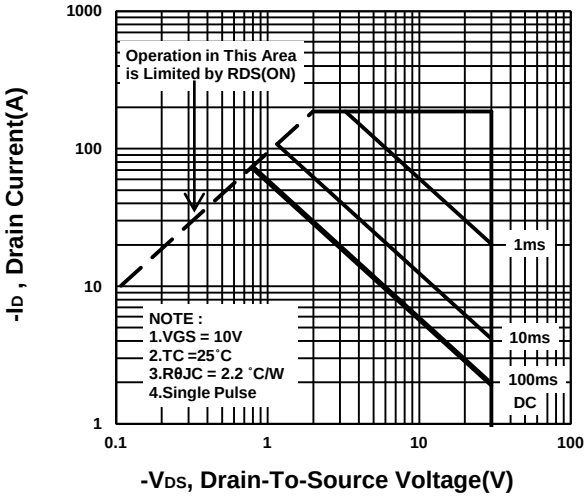
Single Pulse Maximum Power Dissipation



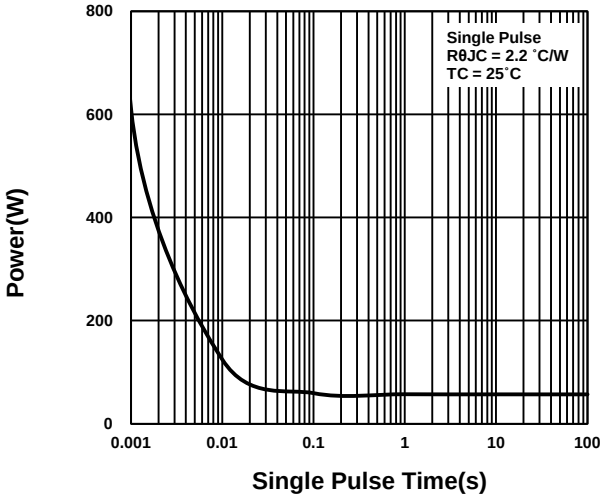
Transient Thermal Response Curve



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve