NIKO-SEM

P-Channel Logic Level Enhancement Mode Field Effect Transistor

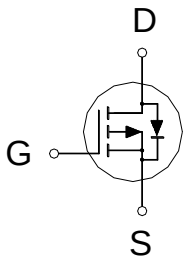
P1203EEA

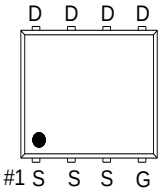
PDFN 3x3P

Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	12mΩ	-40A





G : GATE
D : DRAIN
S : SOURCE

RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current[2]	T_C = 25 °C	I_D	-40	A
	T_C = 100 °C		-25	
	T_A = 25 °C		-11	
	T_A = 70 °C		-9	
Pulsed Drain Current[1]		I_{DM}	-95	
Avalanche Current		I_{AS}	45	
Avalanche Energy	L = 0.1mH	E_{AS}	101	mJ
Power Dissipation	T_C = 25 °C	P_D	31	W
	T_C = 100 °C		12	
	T_A = 25 °C		2.2	
	T_A = 70 °C		1.4	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[3]	Steady-State	$R_{\theta JA}$		55	°C / W
Junction-to-Case	Steady-State	$R_{\theta JC}$		4	

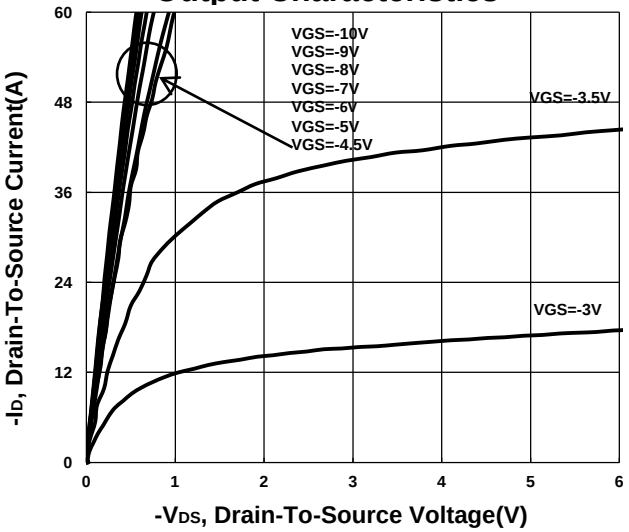
[1]Pulse width limited by maximum junction temperature.
[2]Package limitation current is -30A
[3]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

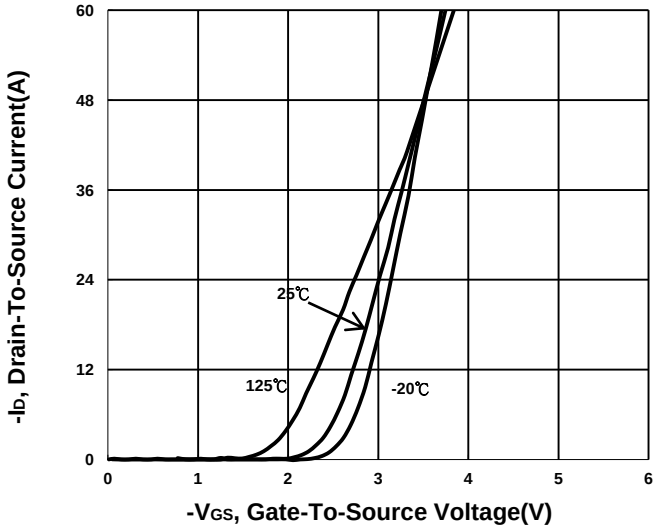
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.5	-2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-95			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -9A		13	19	mΩ
		V_{GS} = -10V, I_D = -12A		8.8	12	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -12A		31		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		2760		pF
Output Capacitance	C_{oss}			437		
Reverse Transfer Capacitance	C_{rss}			395		
Gate Resistance	Rg	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		2.5		Ω
Total Gate Charge[2]	$Q_{g(VGS=10V)}$	V_{DS} = -15V , I_D = -12A		64		nC
	$Q_{g(VGS=4.5V)}$			33		
Gate-Source Charge[2]	Q_{gs}			10		
Gate-Drain Charge[2]	Q_{gd}			16		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -15V, I_D ≅ -12A, V_{GS} = -10V, R_{GS} = 6Ω		21		nS
Rise Time[2]	t_r			25		
Turn-Off Delay Time[2]	$t_{d(off)}$			100		
Fall Time[2]	t_f			73		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current[3]	I_S				-40	A
Forward Voltage[1]	V_{SD}	I_F = -12A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -12A , dI_F/dt = 100 A / μS		21		nS
Reverse Recovery Charge	Q_{rr}			7		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Package limitation current is -30A

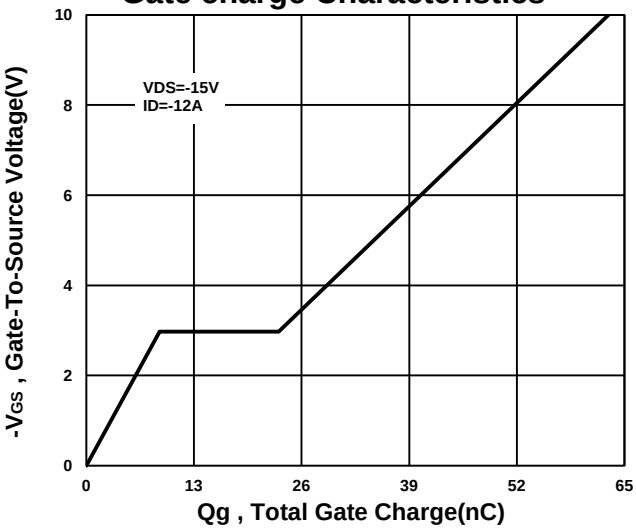
Output Characteristics



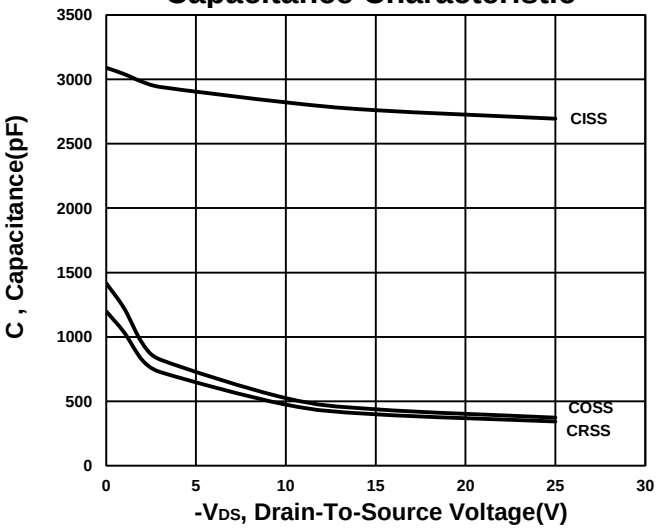
Transfer Characteristics



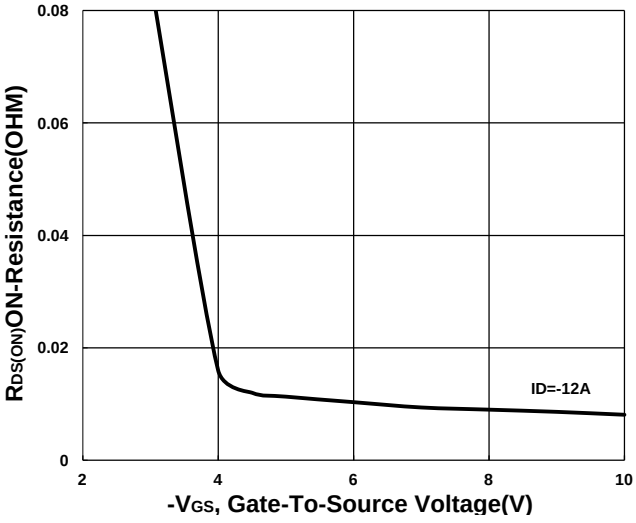
Gate charge Characteristics



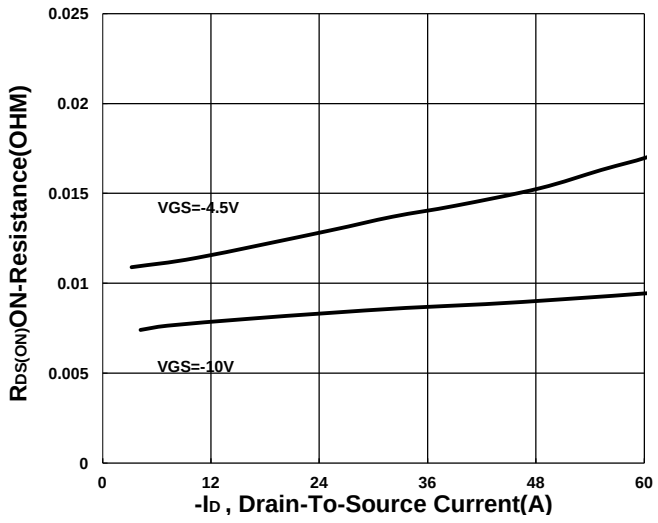
Capacitance Characteristic



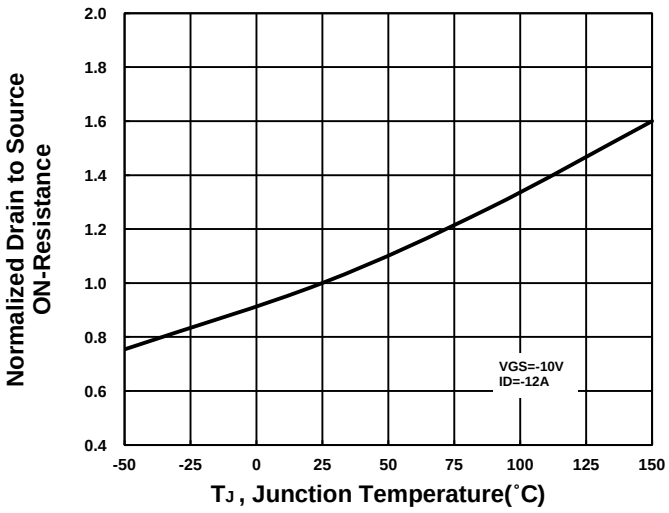
On-Resistance VS Gate-To-Source



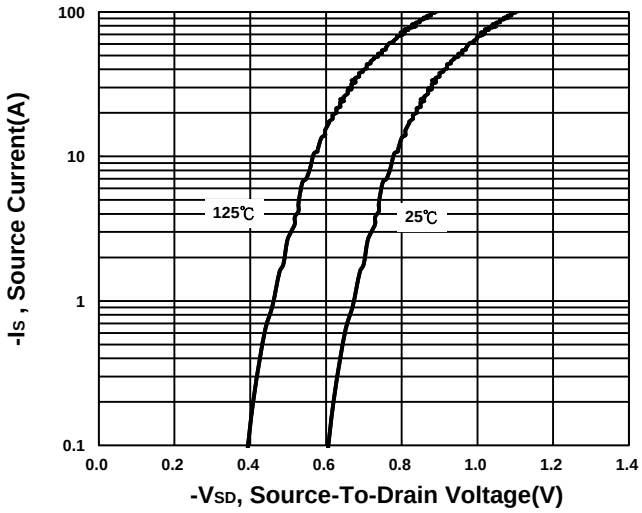
On-Resistance VS Drain Current



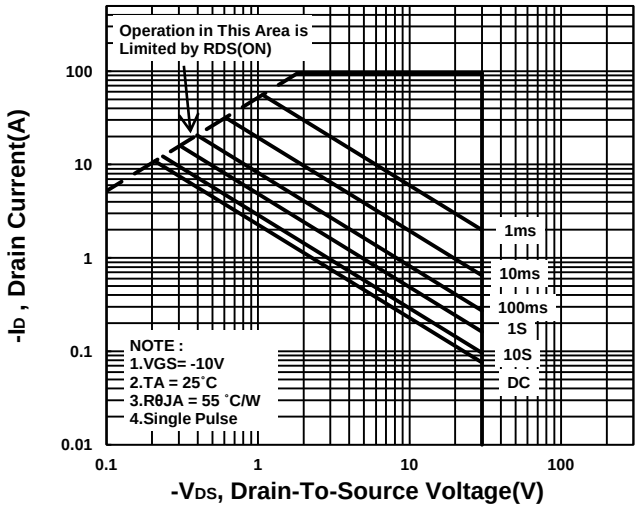
On-Resistance VS Temperature



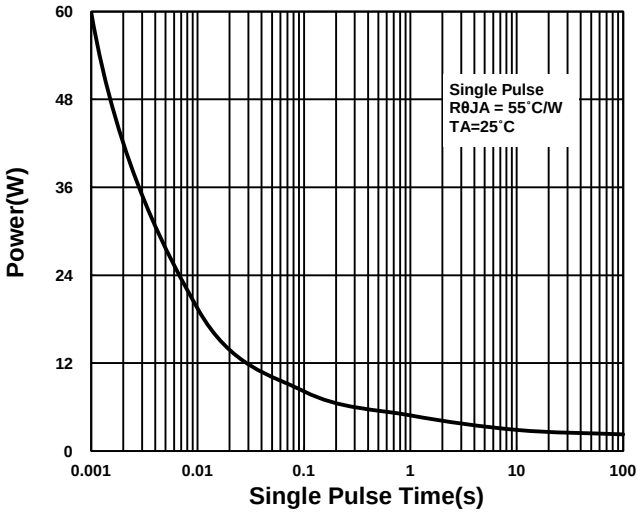
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve