NIKO-SEM

P-Channel Logic Level Enhancement Mode Field Effect Transistor

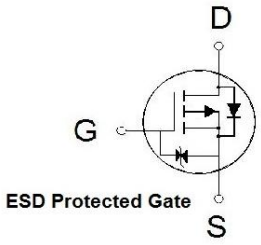
PE5F7EA

PDFN 3x3P

Halogen-free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	13.5mΩ	-35A

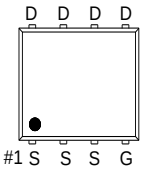


Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- Products Integrated ESD diode with ESD Protected.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



G. GATE
D. DRAIN
S. SOURCE

100% UIS Tested
100% Rg Tested

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C = 25 °C	I_D	-35	A
	T_C = 100 °C		-22	
	T_A = 25 °C		-11	
	T_A = 70 °C		-8.9	
Pulsed Drain Current[1]		I_{DM}	-118	
Avalanche Current		I_{AS}	-40	
Avalanche Energy	L = 0.1mH	E_{AS}	80	mJ
Power Dissipation[3]	T_C = 25 °C	P_D	28	W
	T_C = 100 °C		11	
	T_A = 25 °C		2.8	
	T_A = 70 °C		1.8	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$		45	°C / W
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$		69	
Junction-to-Case	Steady-State	$R_{\theta JC}$		4.5	

[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.

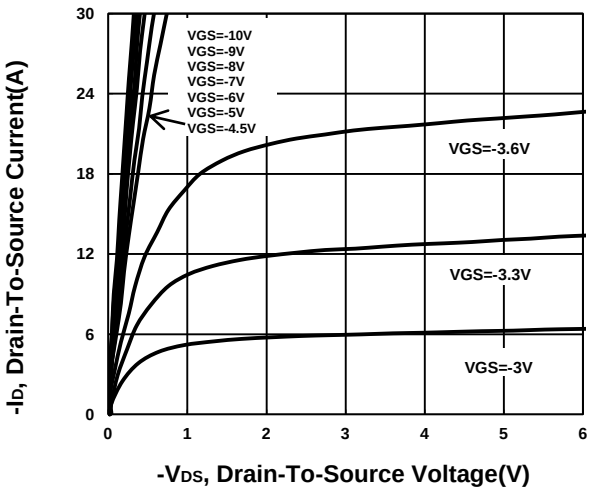
ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.8	-2.3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±30	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	μA
		V_{DS} = -30V, V_{GS} = 0V, T_J = 55 °C			-10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -15A		10.2	13.5	mΩ
		V_{GS} = -4.5V, I_D = -10A		19.5	31.5	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -15A		40		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		1893		pF
Output Capacitance	C_{oss}			310		
Reverse Transfer Capacitance	C_{rss}			262		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		5.8		Ω
Total Gate Charge[2]	$Q_{g(VGS=-10V)}$	V_{DS} = -15V , I_D = -15A		42		nC
	$Q_{g(VGS=-4.5V)}$			21		
Gate-Source Charge[2]	Q_{gs}			6.2		
Gate-Drain Charge[2]	Q_{gd}			12		

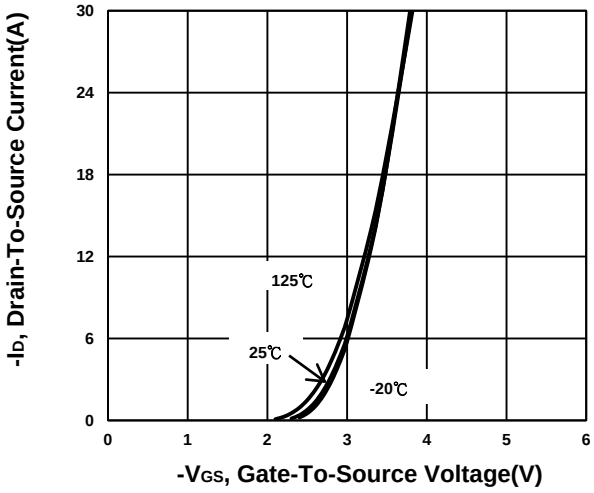
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = -15V $I_D \cong$ -15A, V_{GS} = -10V, R_{GEN} = 6Ω		9.7		nS
Rise Time[2]	t_r			73		
Turn-Off Delay Time[2]	$t_{d(off)}$			80		
Fall Time[2]	t_f			92		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-24	A
Forward Voltage[1]	V_{SD}	I_F = -15A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -15A, dI/dt = 100A/μs		15		nS
Reverse Recovery Charge	Q_{rr}			7.8		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

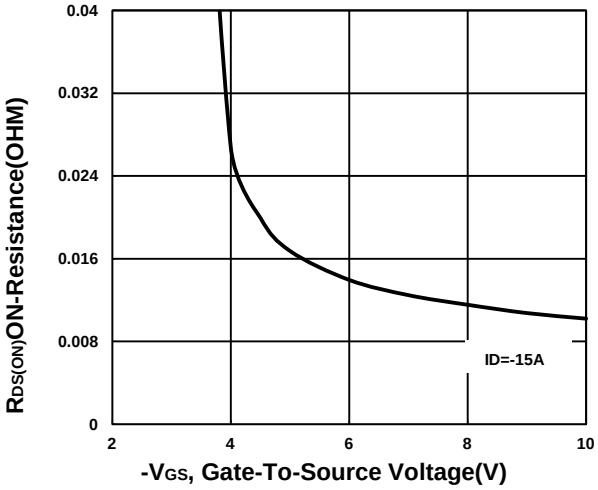
Output Characteristics



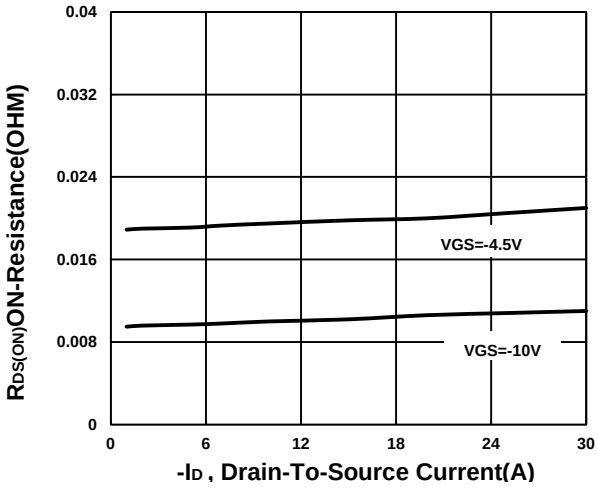
Transfer Characteristics



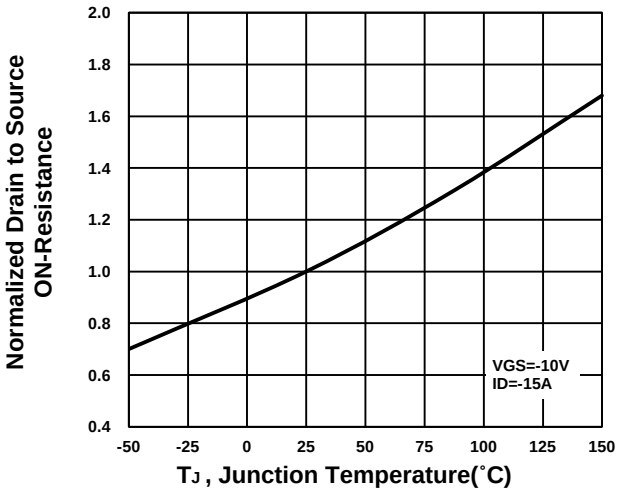
On-Resistance VS Gate-To-Source Voltage



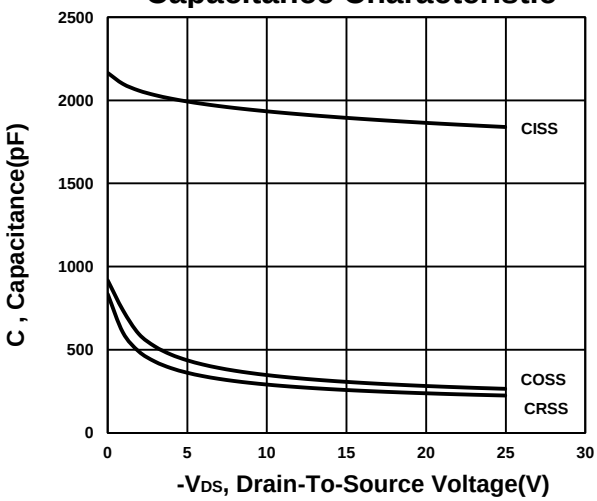
On-Resistance VS Drain Current



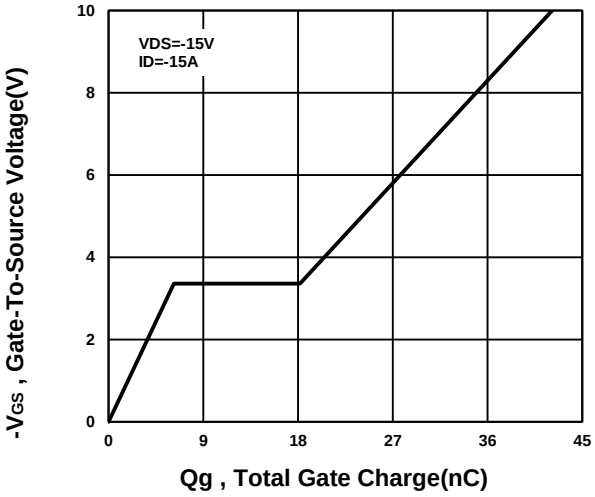
On-Resistance VS Temperature



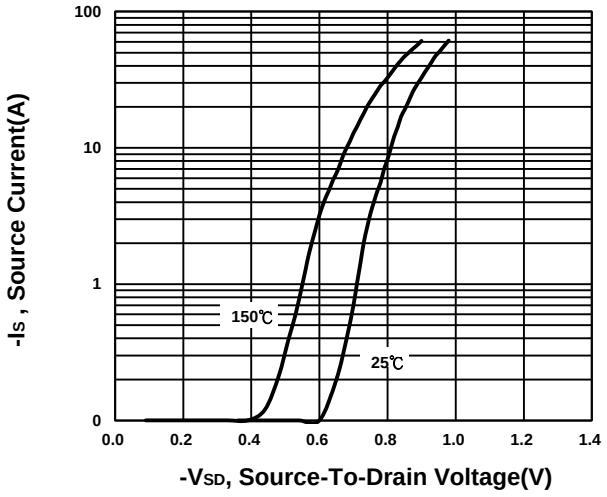
Capacitance Characteristic



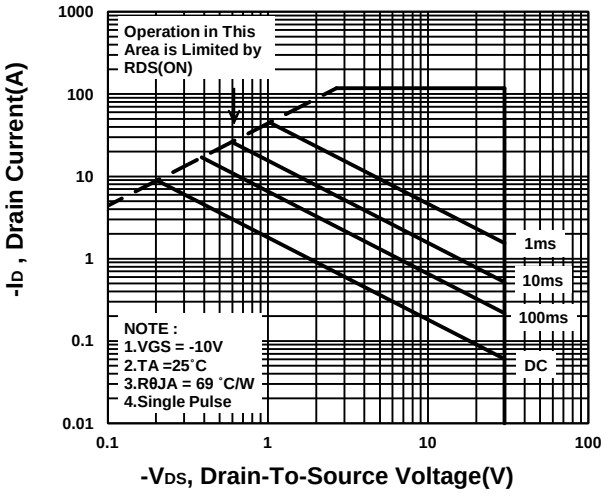
Gate charge Characteristics



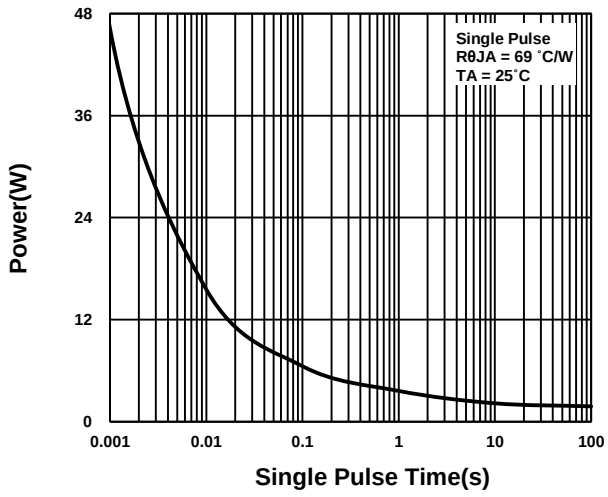
Source-Drain Diode Forward Voltage



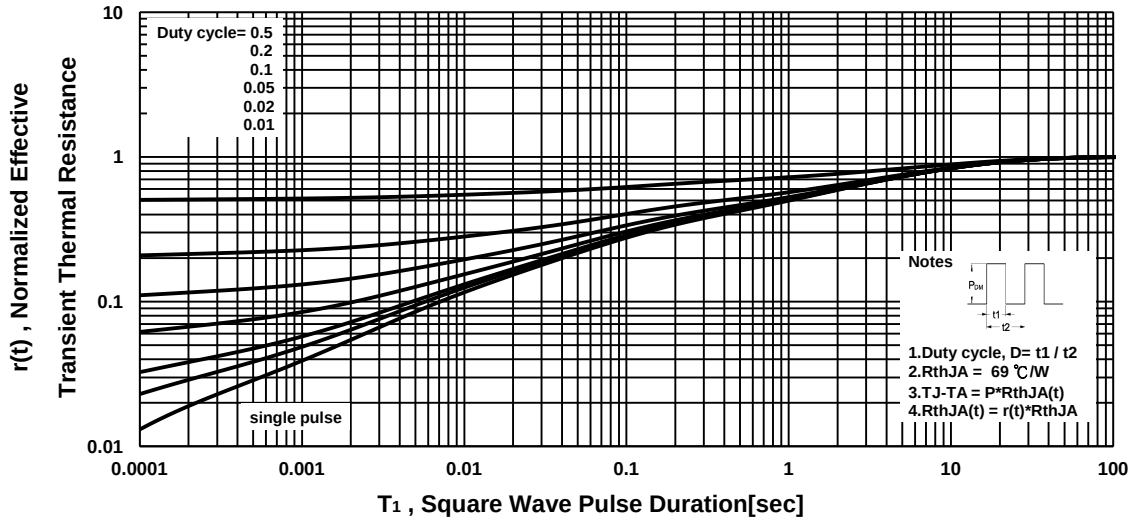
Safe Operating Area



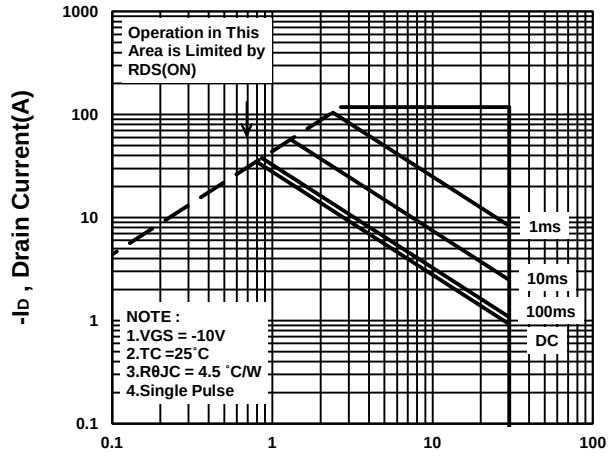
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

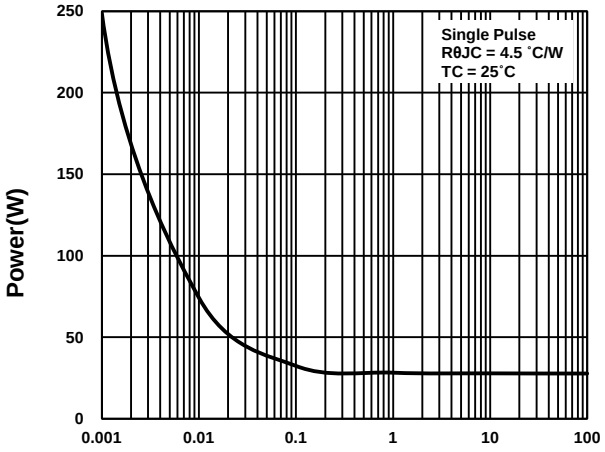


Safe Operating Area



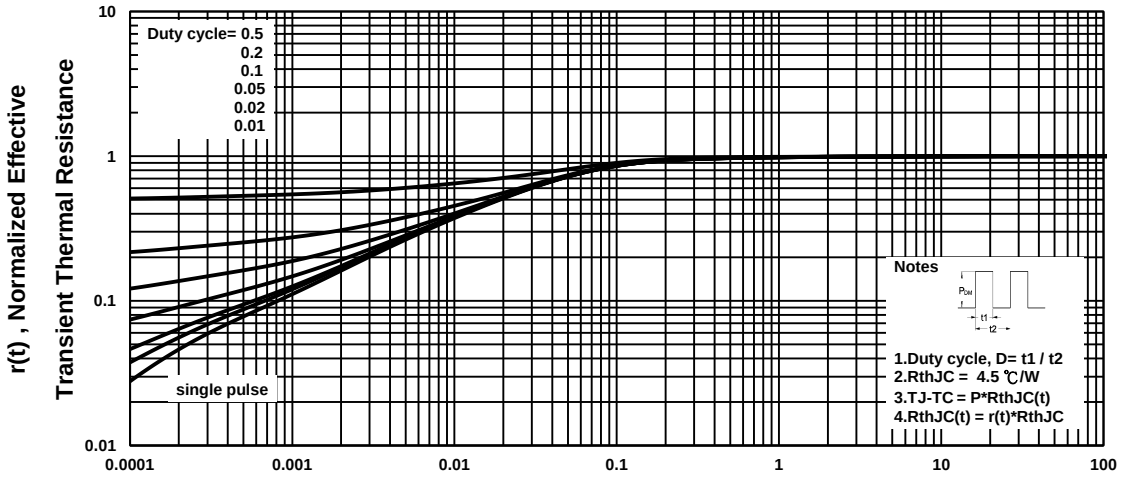
-VDS, Drain-To-Source Voltage(V)

Single Pulse Maximum Power Dissipation



Single Pulse Time(s)

Transient Thermal Response Curve



T1 , Square Wave Pulse Duration[sec]