NIKO-SEM

Dual N-Channel Enhancement Mode Field Effect Transistor

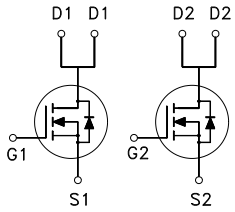
PE6D2DX

PDFN 3x3P

Halogen-Free & Lead-Free

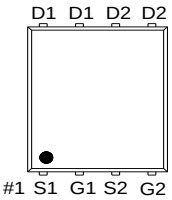
PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
40V	25mΩ	18A



Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.



G : GATE
D : DRAIN
S : SOURCE

Applications

- Protection Circuits Applications.
- Protable Devices for Battery PACK Applications.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	18	A
	T_C = 100 °C		11	
	T_A = 25 °C		6.9	
	T_A = 70 °C		5.5	
Pulsed Drain Current[1]		I_{DM}	30	
Avalanche Current		I_{AS}	14	
Avalanche Energy	L = 0.1mH	E_{AS}	9.8	mJ
Power Dissipation	T_C = 25 °C	P_D	17	W
	T_C = 100 °C		7.1	
	T_A = 25 °C		2.5	
	T_A = 70 °C		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$		50	°C / W
Junction-to-Ambient[2]	Steady-State			90	
Junction-to-Case	Steady-State	$R_{\theta JC}$		7	

[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C

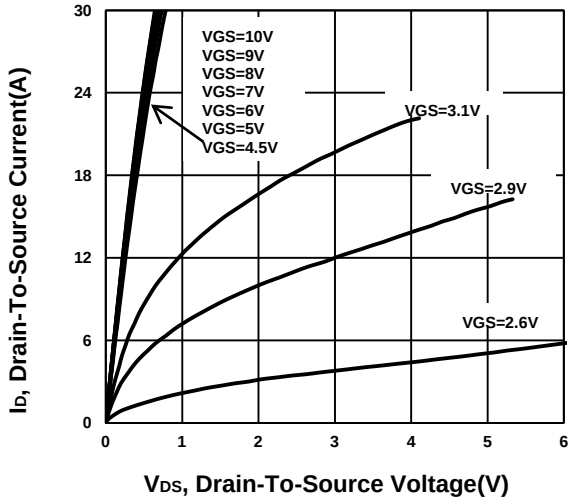
ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.3	1.7	2.3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	μA
		V_{DS} = 40V, V_{GS} = 0V, T_J = 55 °C			10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 6.9A		22	35	mΩ
		V_{GS} = 10V, I_D = 6.9A		19	25	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10V, I_D = 6.9A		28		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1MHz		413		pF
Output Capacitance	C_{oss}			63		
Reverse Transfer Capacitance	C_{rss}			41		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		4.2		Ω
Total Gate Charge[2,3]	$Q_{g(VGS=10V)}$	V_{DS} = 20V , I_D = 6.9A		9.8		nC
	$Q_{g(VGS=4.5V)}$			5.4	7	
Gate-Source Charge[2,3]	Q_{gs}			1		
Gate-Drain Charge[2,3]	Q_{gd}			3.1		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 0V I_D ≅ 6.9A, V_{GEN} = 10V, R_G =6Ω		6		nS
Rise Time[2]	t_r			65		
Turn-Off Delay Time[2]	$t_{d(off)}$			17		
Fall Time[2]	t_f			101		

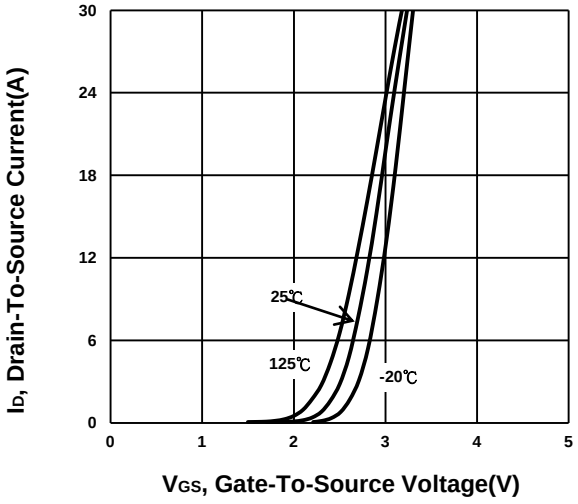
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current[3]	I_S				13	A
Forward Voltage[1]	V_{SD}	I_F = 6.9A, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 6.9A , dI_F/dt = 100A / μS		3.3		nS
Reverse Recovery Charge	Q_{rr}			1		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Guaranteed by design, not subject to production testing

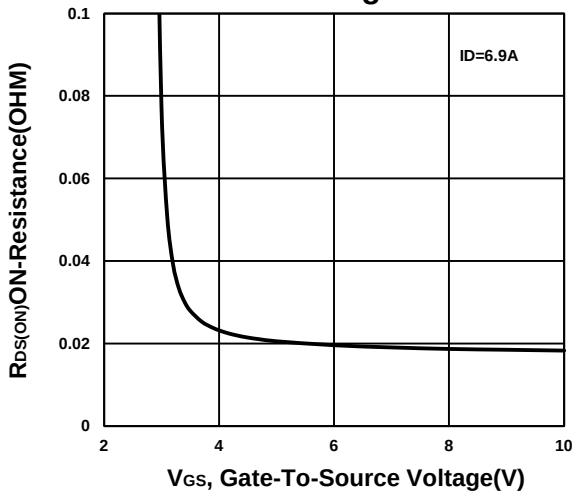
Output Characteristics



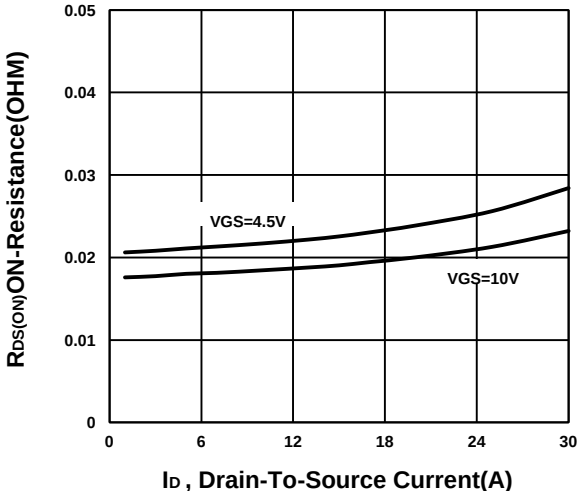
Transfer Characteristics



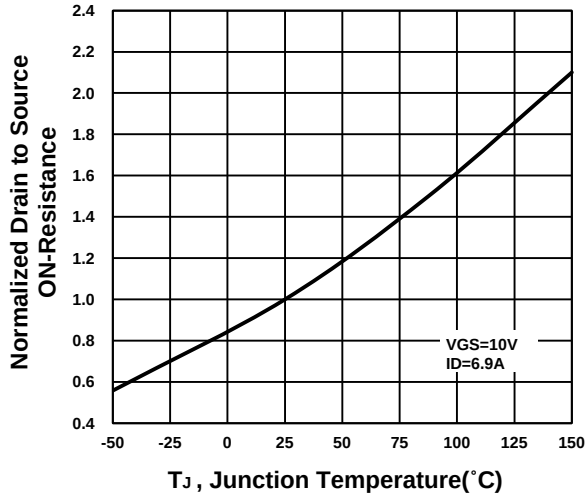
On-Resistance VS Gate-To-Source Voltage



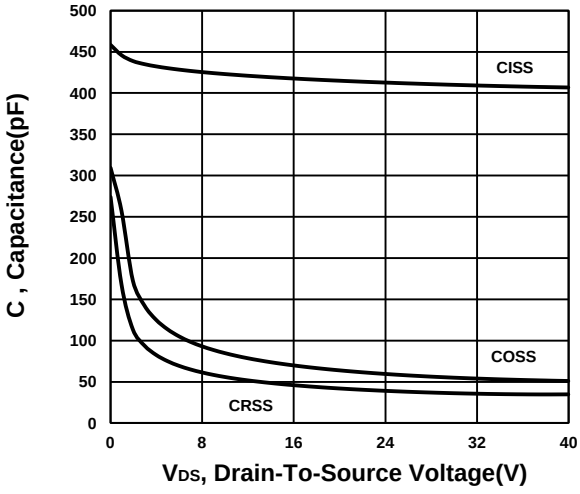
On-Resistance VS Drain Current



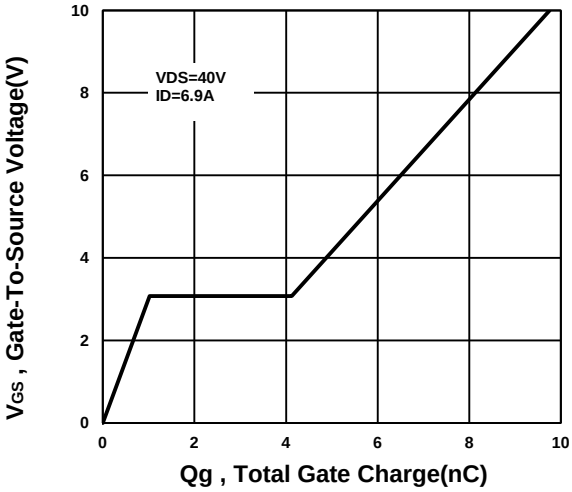
On-Resistance VS Temperature



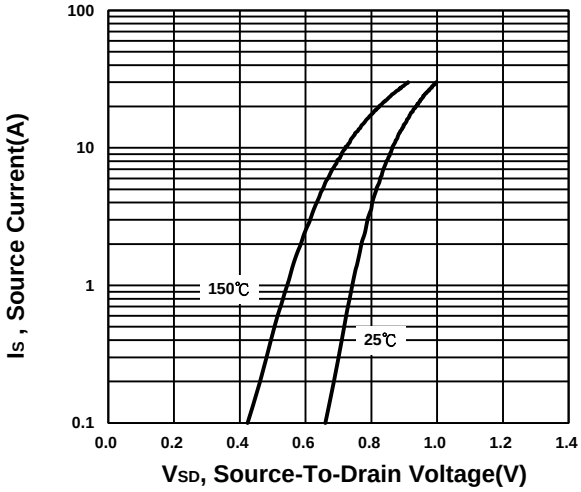
Capacitance Characteristic



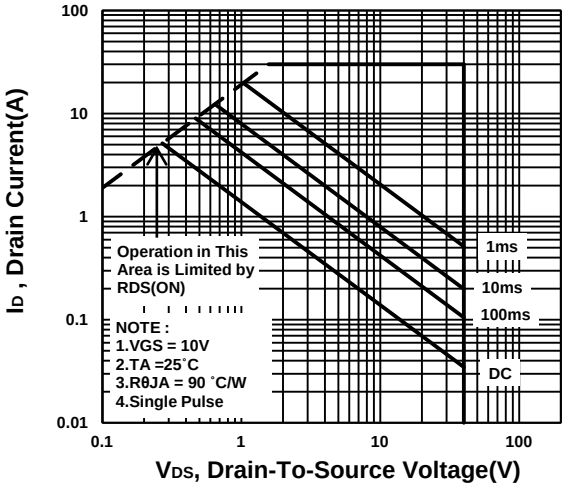
Gate charge Characteristics



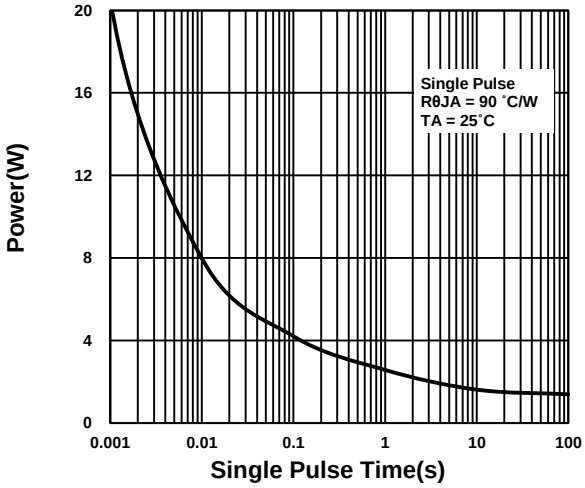
Source-Drain Diode Forward Voltage



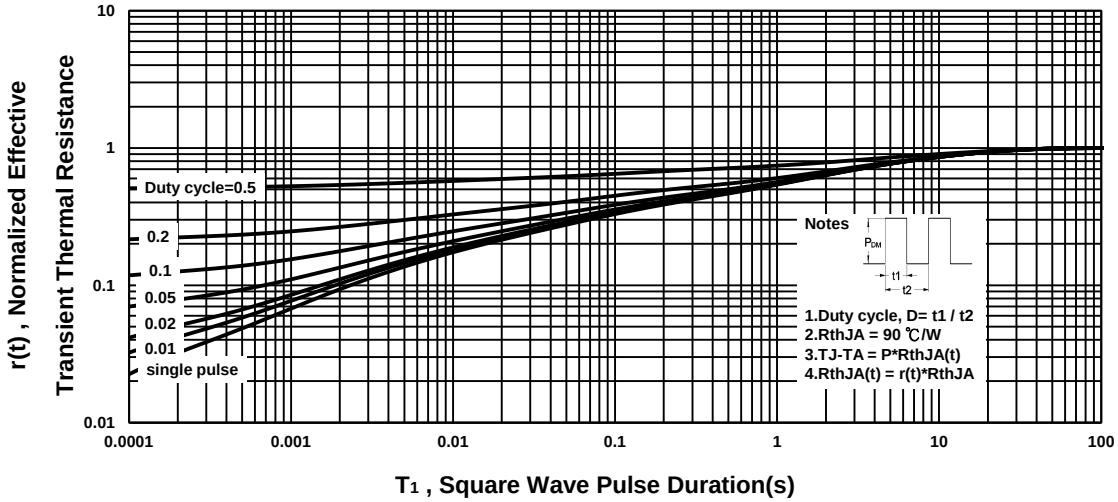
Safe Operating Area



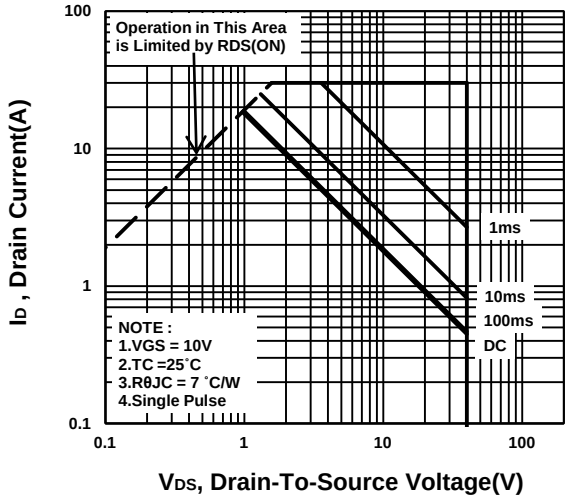
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Safe Operating Area



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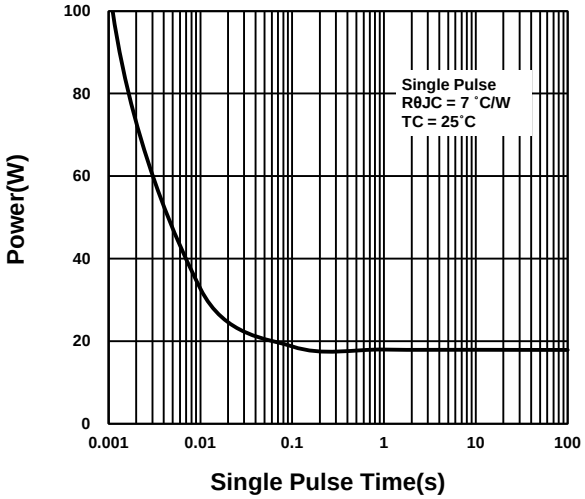

Transient Thermal Response Curve