NIKO-SEM

Dual N-Channel Enhancement Mode Field Effect Transistor

PE848DU

PDFN 3.3x3.3S

Halogen-Free & Lead-Free

PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
Q2	30V	5.8mΩ	18A
Q1	30V	4.2mΩ	21A

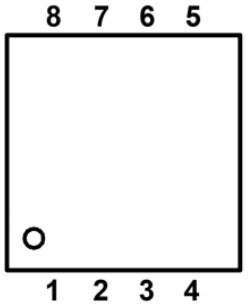
RoHS Compliant

Features

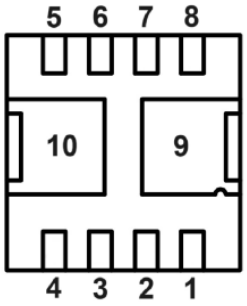
- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- 100% UIS and Rg Tested.

Applications

- Computing DC to DC converters.
- Communications DC to DC converters.
- General Purpose Point of load.



Top



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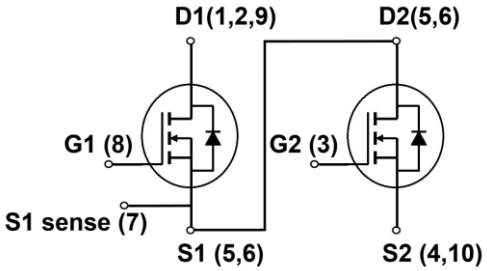


PINNING INFORMATION

PIN	SYMBOL	DESCRIPTION
1,2,9	D1	Drain 1
3	G2	Gate 2
4,10	S2	Source 2
5,6	D2 / S1	Drain 2 / Source 1
7	S1	Source sense 1
8	G1	Gate 1

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	Q2	Q1	UNITS
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current	T_C = 25 °C	I_D	50	50	A
	T_C = 100 °C		33	42	
Pulsed Drain Current[1]		I_{DM}	88	110	
Continuous Drain Current[3]	T_A = 25 °C	I_D	18	21	
	T_A = 70 °C		14	17	
Avalanche Current[4]		I_{AS}	31	42	
Avalanche Energy[4]		E_{AS}	14	26	mJ
Power Dissipation	T_C = 25 °C	P_D	27	33	W
	T_C = 100 °C		11	13	
Power Dissipation[3]	T_A = 25 °C	P_D	3.1	3.4	W
	T_A = 70 °C		2	2.2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL		TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$	Q2		40	°C / W
			Q1		36	
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$	Q2		66	
			Q1		63	
Junction-to-Case		$R_{\theta JC}$	Q2		4.5	
			Q1		3.8	

[1]Pulse width limited by maximum junction temperature $T_{J(MAX)}$=150°C.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.
[4]VDD=50V, L=0.03mH, Rg=25Ω.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q2	30			V
		V_{GS} = 0V, I_D = 250μA	Q1	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q2	1.2	1.6	2.2	
		V_{DS} = V_{GS}, I_D = 250μA	Q1	1.2	1.6	2.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V	Q2			±100	nA
		V_{DS} = 0V, V_{GS} = ±12V	Q1			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	Q2			1	μA
		V_{DS} = 30V, V_{GS} = 0V	Q1			1	
		V_{DS} = 30V, V_{GS} = 0V, T_J = 55 °C	Q2			10	
		V_{DS} = 30V, V_{GS} = 0V, T_J = 55 °C	Q1			10	
Drain-Source On-State Resistance[5]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 18A	Q2		4	5.8	mΩ
		V_{GS} = 10V, I_D = 20A	Q1		2.9	4.2	
		V_{GS} = 4.5V, I_D = 18A	Q2		5.8	7.8	
		V_{GS} = 4.5V, I_D = 20A	Q1		4.1	5.7	
Forward Transconductance[5]	g_{fs}	V_{DS} = 5V, I_D = 18A	Q2		60		S
		V_{DS} = 5V, I_D = 20A	Q1		85		
DYNAMIC							
Input Capacitance	C_{iss}	Q2 V_{GS} = 0V, V_{DS} = 15V f = 1MHz Q1 V_{GS} = 0V, V_{DS} = 15V f = 1MHz	Q2		770		pF
			Q1		1216		
Output Capacitance	C_{oss}		Q2		208		
			Q1		294		
Reverse Transfer Capacitance	C_{rss}		Q2		42		
			Q1		47		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	Q2		1.1		Ω
			Q1		1.6		
Total Gate Charge[6]	Q_g VGS = 10V	Q2 V_{DS} = 15V V_{GS} = 10V, I_D = 18A Q1 V_{DS} = 15V V_{GS} = 10V, I_D = 20A	Q2		14	20	nC
			Q1		19.7	28	
	Q_g VGS = 4.5V		Q2		7.6	11	
			Q1		9.9	14	
Gate-Source Charge[6]	Q_{gs}		Q2		1.8		
			Q1		3.2		
Gate-Drain Charge[6]	Q_{gd}		Q2		2.9		
			Q1		3.5		

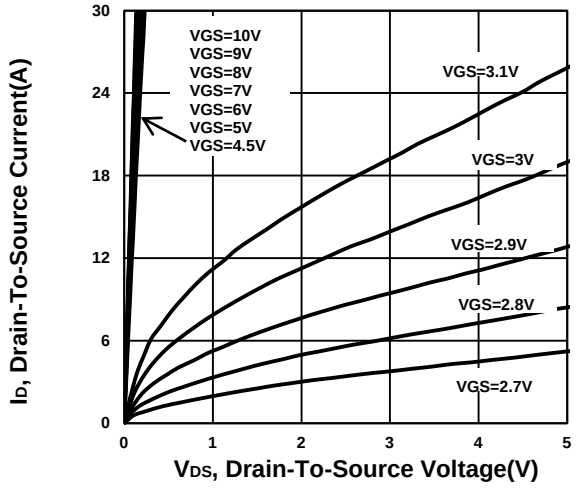
Turn-On Delay Time[6]	$t_{d(on)}$	Q2 , V_{DS} = 15V $I_D \cong$ 18A V_{GS} = 10V, R_{GEN} =6Ω	Q2		7.4		nS
			Q1		9.2		
Rise Time[6]	t_r		Q2		64		
			Q1		70		
Turn-Off Delay Time[6]	$t_{d(off)}$	Q1 , V_{DS} = 15V $I_D \cong$ 20A, V_{GS} = 10V, R_{GEN} =6Ω	Q2		20		
			Q1		29		
Fall Time[6]	t_f		Q2		73		
			Q1		92		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current	I_S		Q2			27	A
			Q1			27	
Forward Voltage[5]	V_{SD}	I_F = 18A V_{GS} = 0V	Q2			1	V
		I_F = 20A, V_{GS} = 0V	Q1			1.2	
Reverse Recovery Time	t_{rr}	Q2 I_F = 18A dI_F/dt = 400A / μS	Q2		12		nS
			Q1		14		
Reverse Recovery Charge	Q_{rr}	Q1 I_F = 20A, dI_F/dt = 400A / μS	Q2		10		nC
			Q1		17		

[5]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[6]Independent of operating temperature.

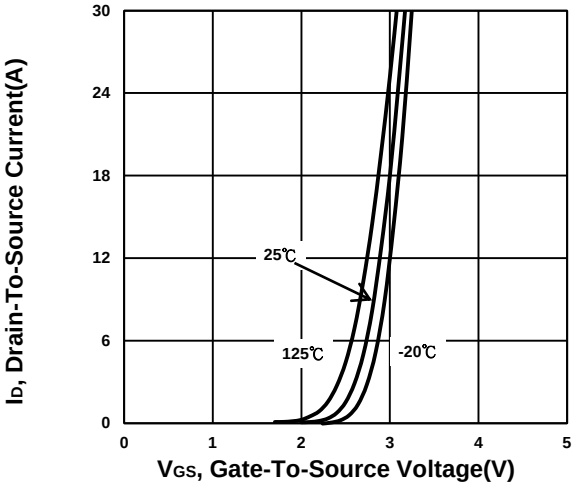
TYPICAL PERFORMANCE CHARACTERISTICS

Q2

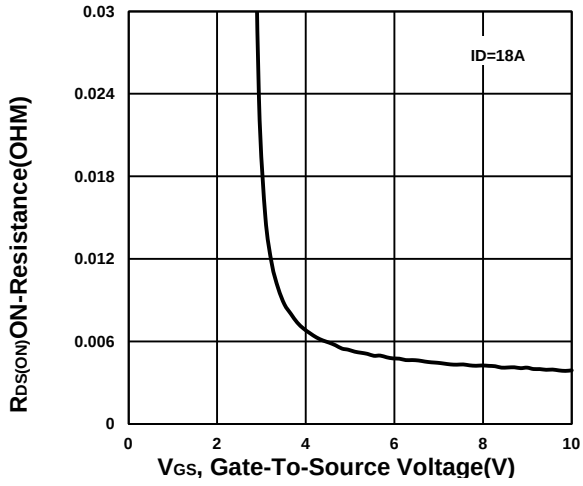
Output Characteristics



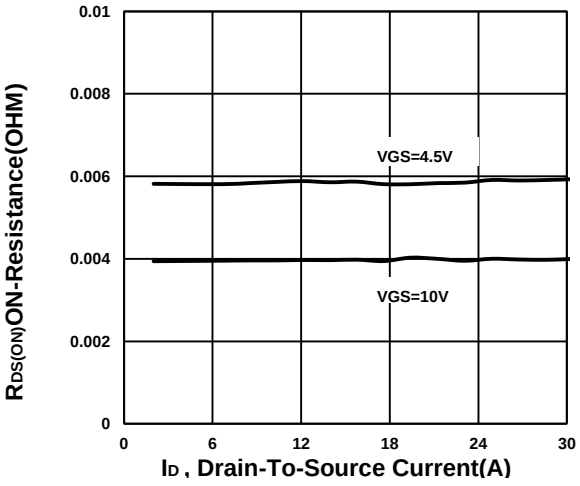
Transfer Characteristics



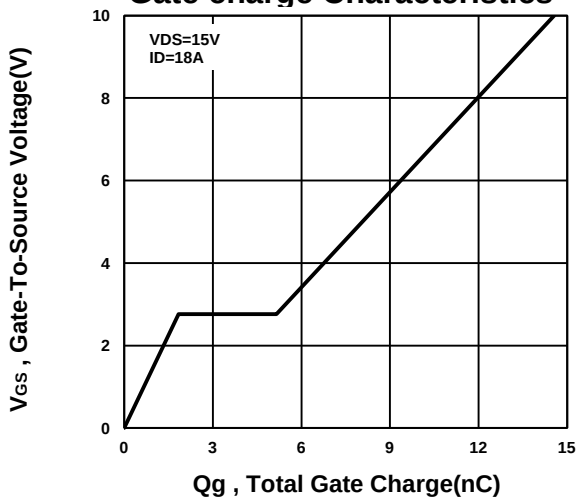
On-Resistance VS Gate-To-Source Voltage



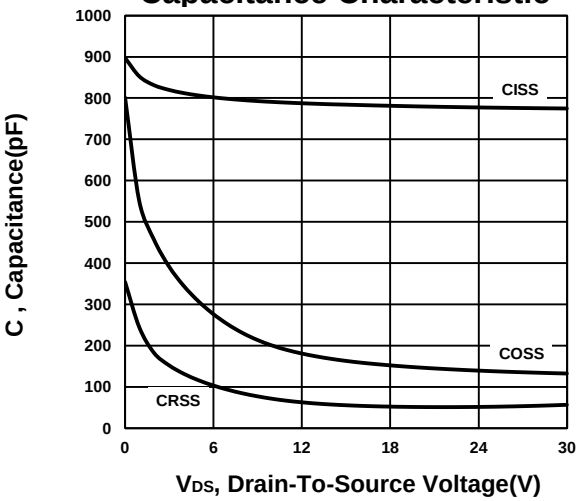
On-Resistance VS Drain Current



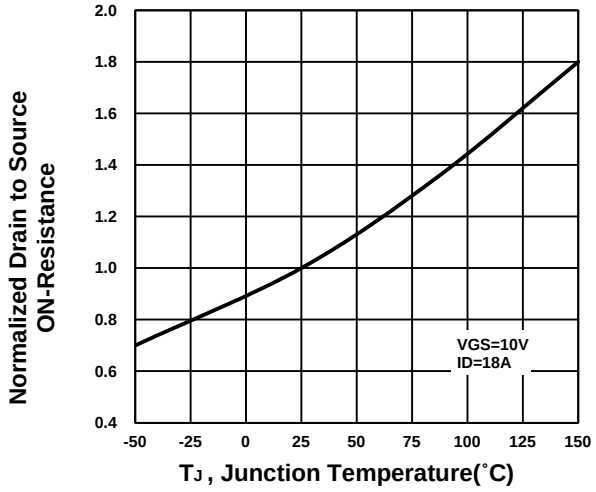
Gate charge Characteristics



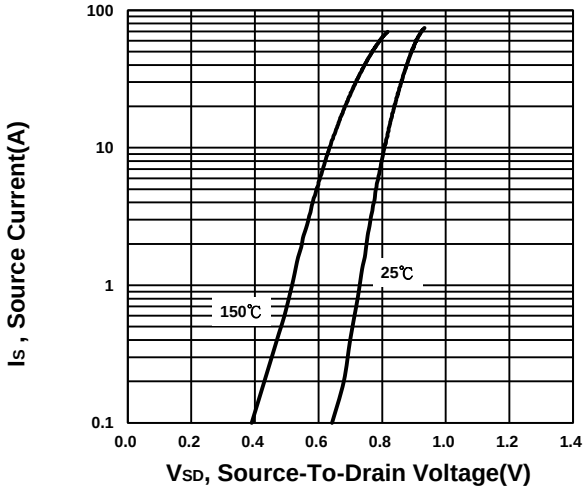
Capacitance Characteristic



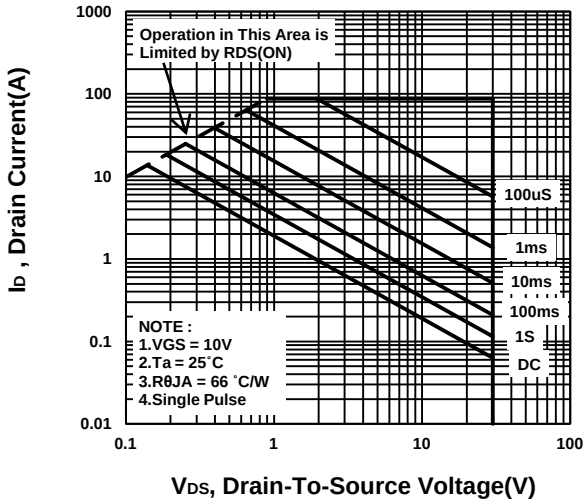
On-Resistance VS Temperature



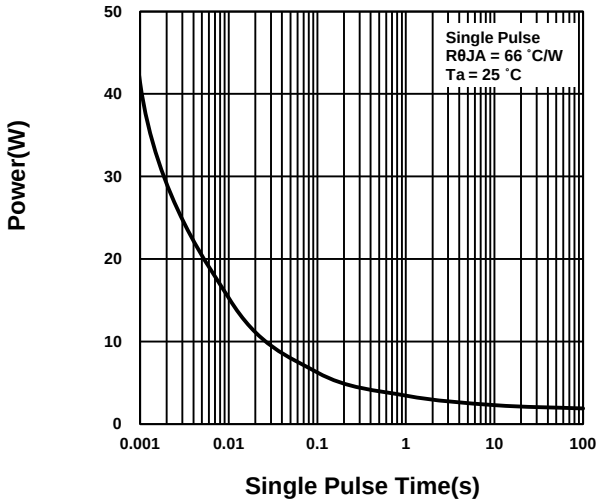
Source-Drain Diode Forward Voltage



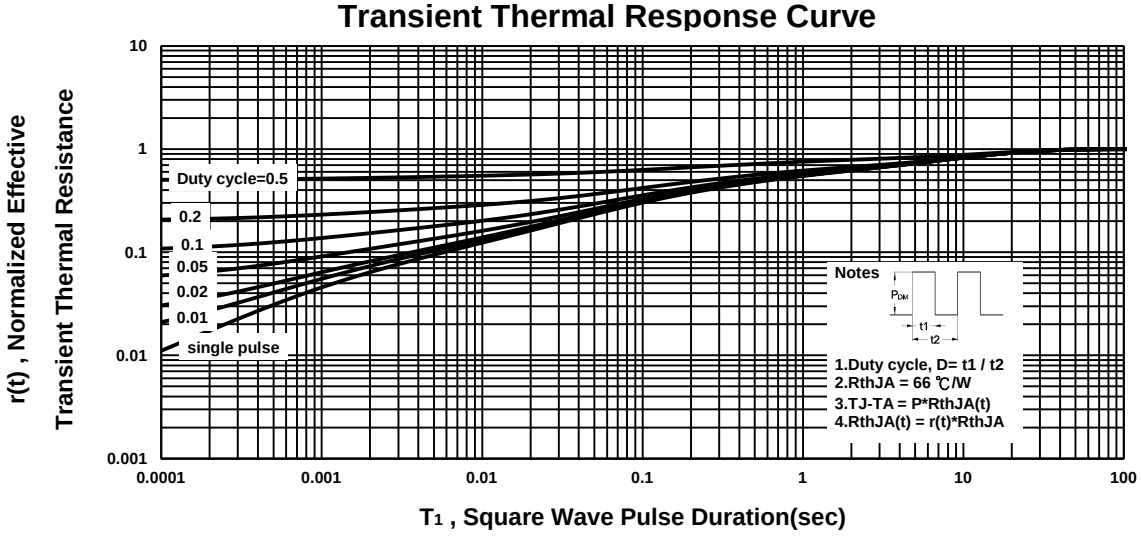
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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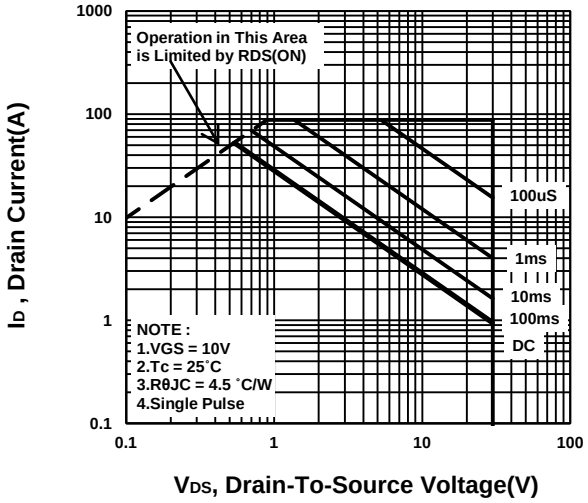

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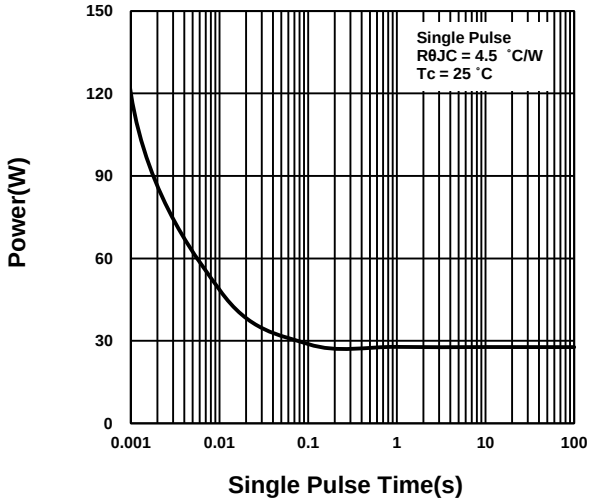

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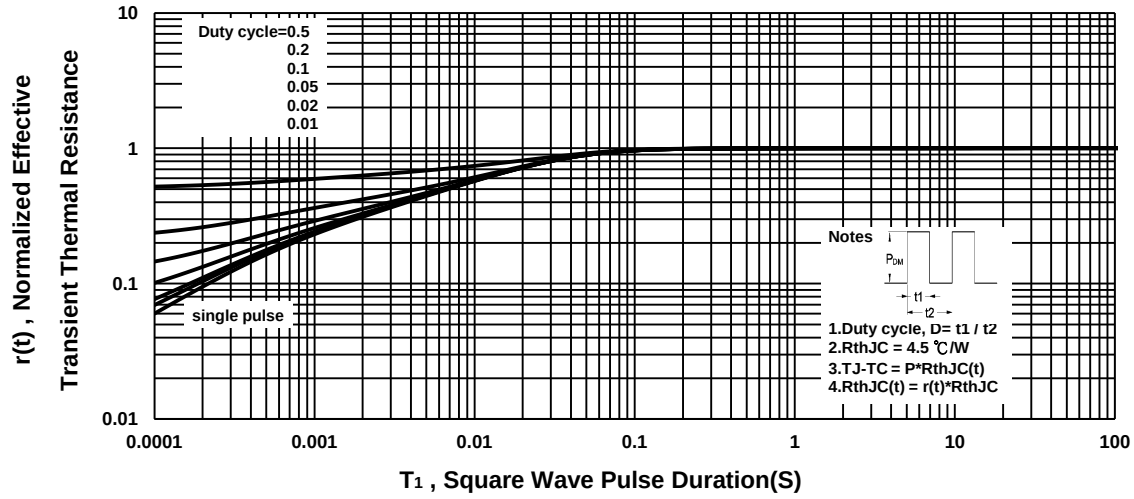
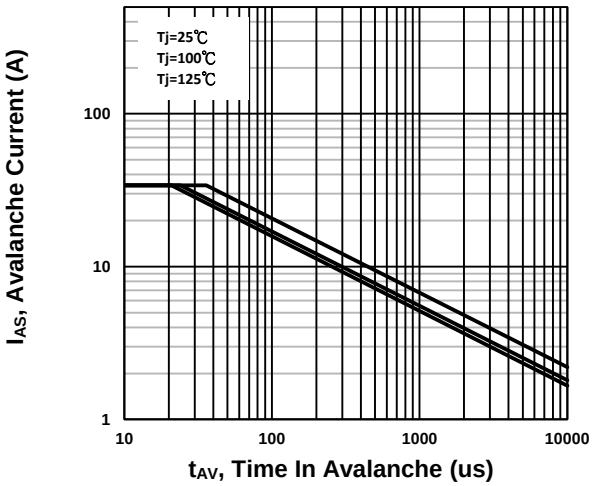
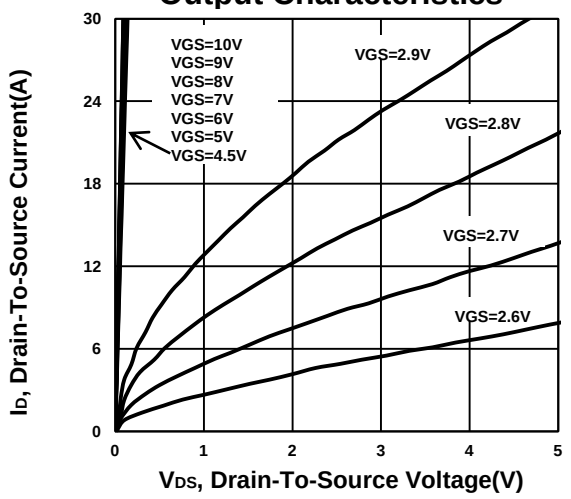


Unclamped Inductive Switching Capability

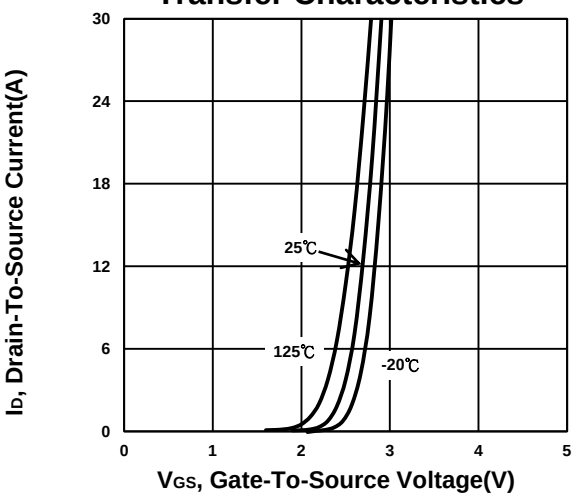


Q1

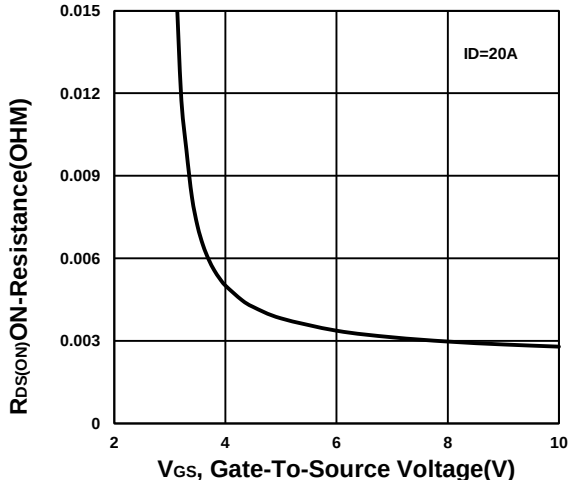
Output Characteristics



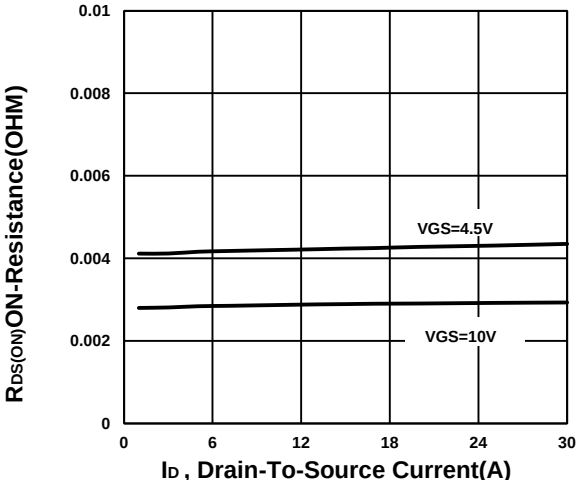
Transfer Characteristics



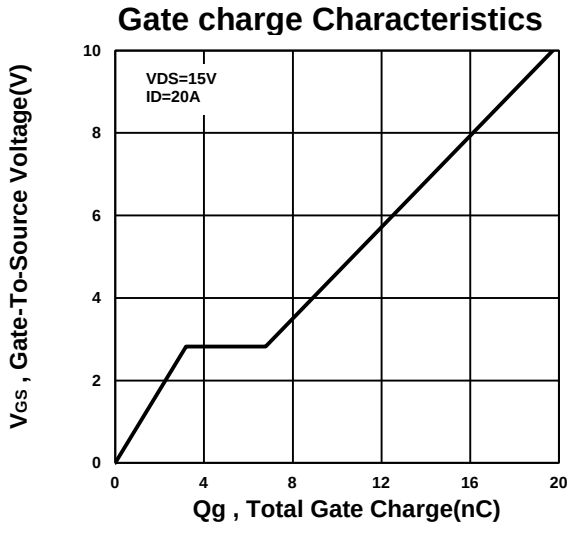
On-Resistance VS Gate-To-Source Voltage



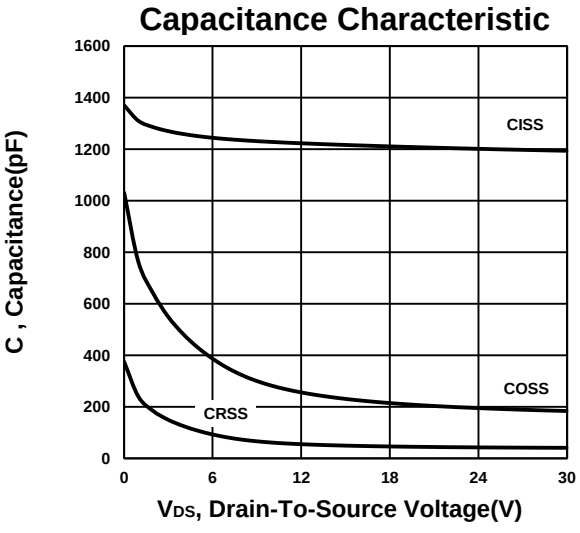
On-Resistance VS Drain Current



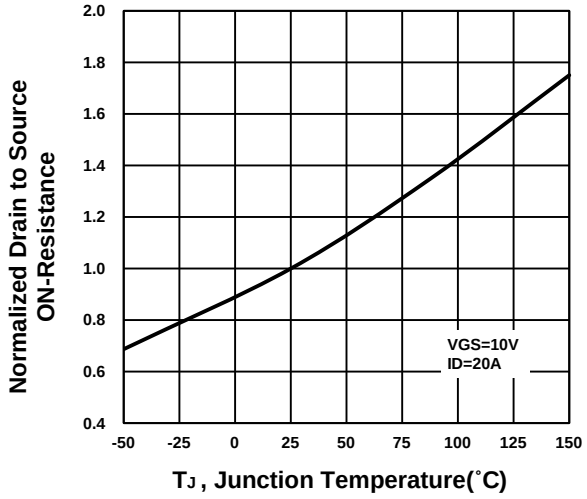
Gate charge Characteristics



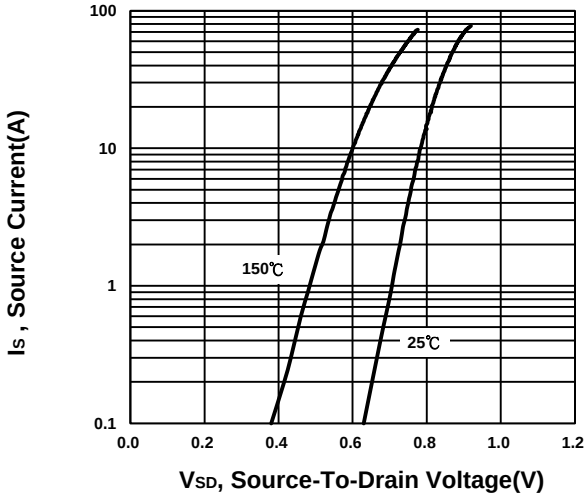
Capacitance Characteristic



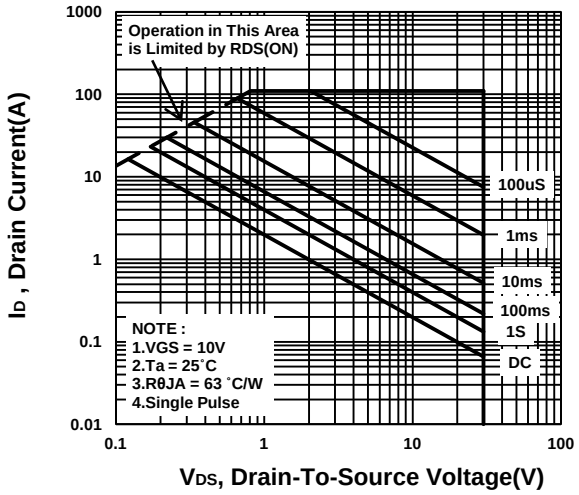
On-Resistance VS Temperature



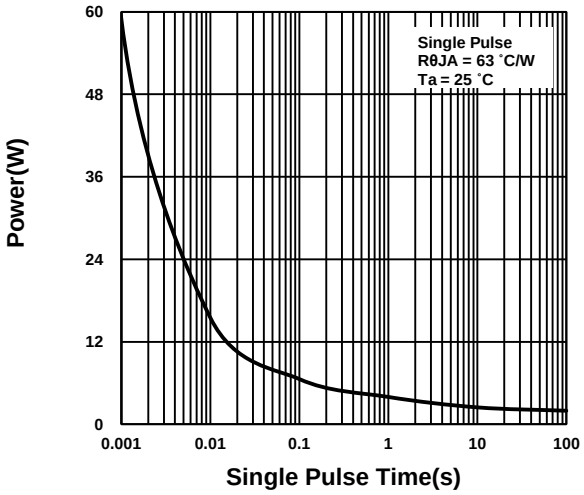
Source-Drain Diode Forward Voltage



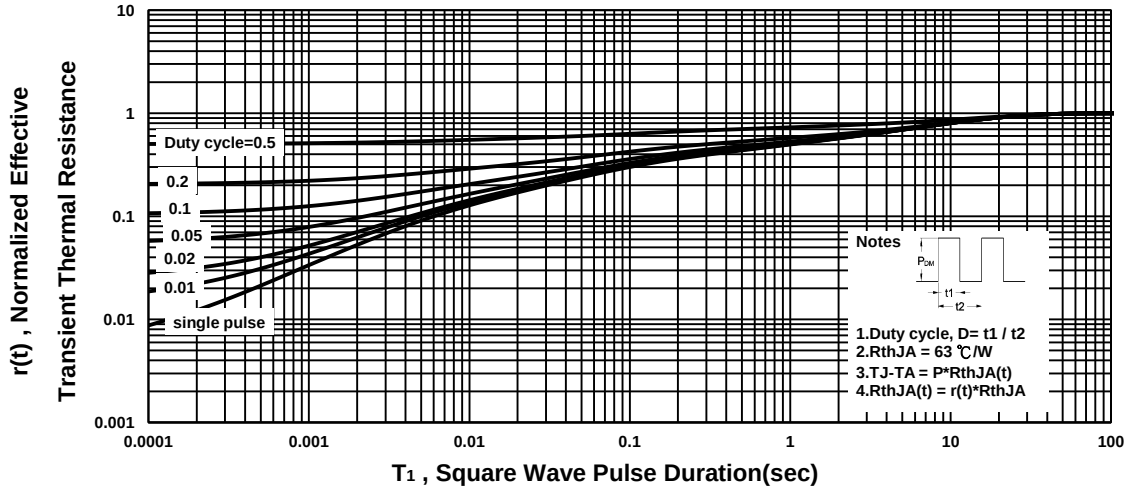
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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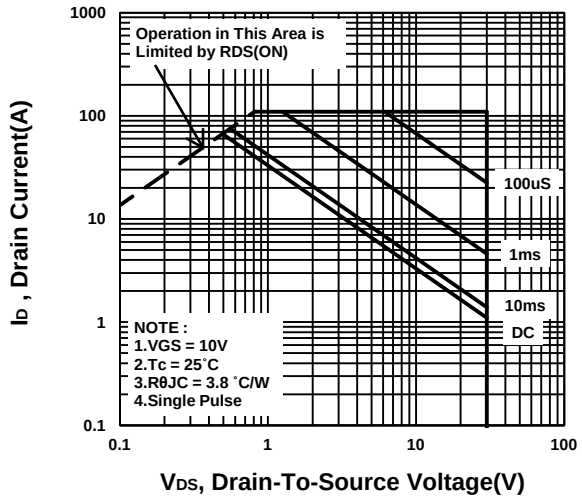

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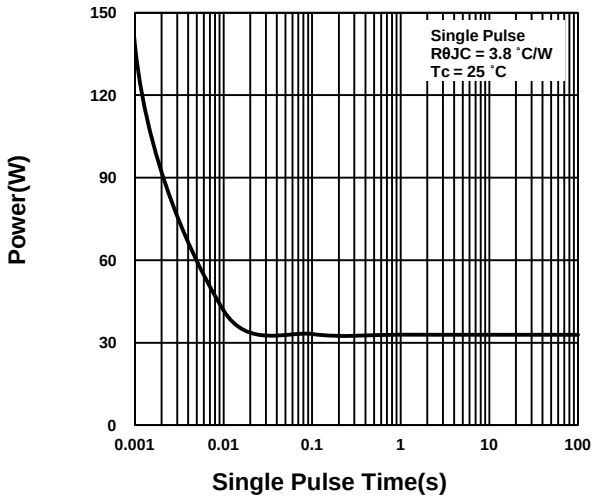

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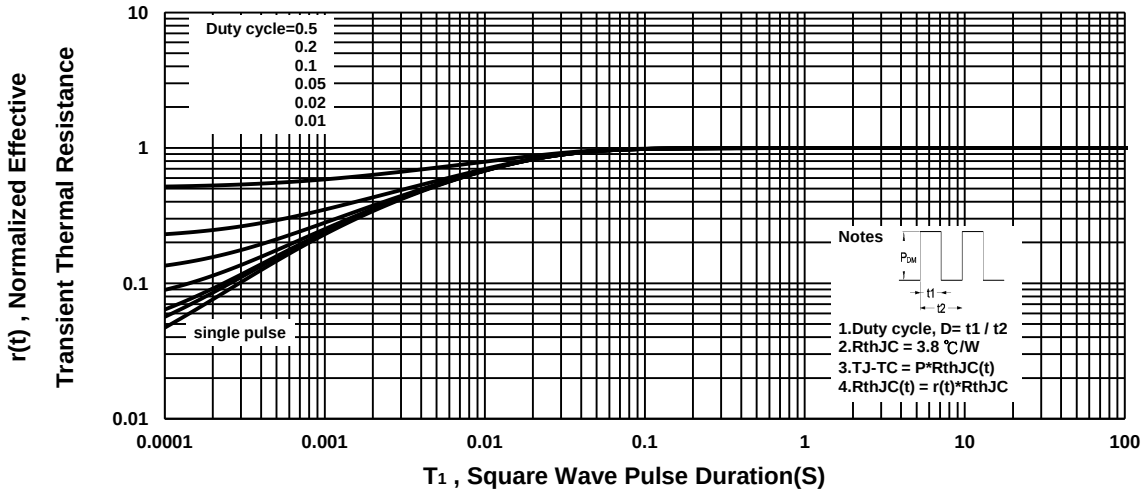

Unclamped Inductive Switching Capability